KIT – Kalaignarkarunanidhi Institute of Technology

(An Autonomous Institution)

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
Accredited by NAAC with 'A' GRADE & NBA (CSE, ECE, EEE, MECH)
An ISO 9001 : 2015 Certified Institution
Coimbatore – 641 402.

REGULATIONS, CURRICULUM & SYLLABUS – 2019

(Applicable for students admitted from the Academic Year 2019-20 onwards)

I to IV Semester

DEGREE OF MASTER OF ENGINEERING
IN
VLSI DESIGN

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

Vision	
◎	To impart standard education, training and research in the field of Electronics and Communication Engineering and to produce globally proficient engineers.

Mission	
◎	Provide quality and contemporary education in the domain of ECE to produce globally competitive engineers.
◎	Facilitates industry institution interaction in teaching & learning, consultancy and research activities to accomplish the technological needs of the society.
◎	Develop entrepreneurship qualities and good management practices by adhering to the professional ethical code.

Program Educational Objectives (PEO's)	
PEO 1	Graduates will be able to design VLSI based innovative products and provide solutions to all the societal needs.
PEO 2	Graduates will undertake research in the VLSI domain with high level of technical knowledge and lifelong learning.
PEO 3	Graduates will be able to demonstrate professional, ethical and social responsibility and engage themselves in perpetual learning to suit multi-disciplinary teams.

Programme Outcomes (PO's)	
After the successful completion of the P.G. programme in VLSI Design, Graduates will be able to:	
PO 1	**Engineering knowledge :** Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem analysis :** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
PO 3	**Design / development of solutions :** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety and the cultural, societal, and environmental considerations.

PO 4	**Conduct investigations of complex problems :** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage :** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The Engineer and society :** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability :** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics :** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	**Individual and team work :** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication :** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO 11	**Project management and finance :** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning :** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcome (PSO's)	
After the successful completion of the P.G. programme in VLSI Design, Graduates will be able to:	
PSO 1	Analyze various techniques for the innovative design of VLSI based applications.
PSO 2	Test the performance of VLSI based applications through specific tools for VLSI.

PG Regulations

1. SHORT TITLE AND COMMENCEMENT

- These Regulations shall be called the "KIT-Kalaignarkaraunanidhi Institute of Technology, Coimbatore, Regulations for the Award of M.E. / M.B.A / M.C.A., Degree".
- They have been evolved, drafted and implemented after deliberations in and approvals from UGC, Anna University and Academic Council of the Institute, and are subject to change / modifications from time to time; (major modifications at a frequency of FOUR years in synchronization with the curriculum structure revision and minor changes as and when applicable).
- The latest/first version shall be applicable for the students enrolling for M.E. / M.B.A / M.C.A., degree programs at this Institute from Academic year 2019-2020 onwards.

2. PREAMBLE

The regulations prescribed herein have been made by KIT, an autonomous institution, approved by AICTE,New Delhi and affiliated to the Anna University, Chennai, to facilitate the smooth and orderly conduct of its academic programmes and activities at the M.E. / M.B.A / M.C.A. level. It is expected that the regulations will enable the students to take advantage of the various academic opportunities at the Institute and prepare themselves to face the challenges in their professional careers ahead. It may be noted that :

a. The provision made herein shall be applicable to all the M.E./M.B.A/M.C.A.,. programmes offered at the institute, at present;

b. They shall also be applicable to all the new M.E./M.B.A/M.C.A., programmes which may be started at the Institute in the future;

c. Academic and non-academic requirements prescribed by the Academic Council have to be fulfilled by a student for eligibility towards award of M.E. / M.B.A / M.C.A., Degree.

3. PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires :

Sl. No.	Name	Definition
1.	**Programme**	Refers to Degree Programme that is B.E./B.Tech. Degree Programme.
2.	**Discipline**	Refers to branch or specialization of B.E./B.Tech. Degree Programme, like Computer Science and Engineering, Mechanical Engineering etc.,
3.	**Course**	Refers to a theory or practical subject that is normally studied in a semester, like Mathematics, Physics, etc.,
4.	**Head of the Institution**	Refers to the Principal of the College.

5.	**Controller of Examinations (CoE)**	Refers to the authority of the college who is responsible for all activities of the Examinations.
6.	**Head of the Department (HoD)**	Refers to the Head of the Department concerned.
7.	**University**	Refers to Anna University, Chennai.
8.	**College (KIT)**	Refers to KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore.
9.	**Curriculum**	Refers to the various components/courses studied in each programme that provide appropriate outcomes (knowledge, skill and behavior/attitude) in the chosen branch of study.
10.	**T-P-TU- C**	Refers to Theory, Practical, Tutorial and Credits respectively.
11.	**Foundation Courses (FC)**	May include Mathematics or other basic courses
12.	**Professional Core (PC)**	Courses include the core courses relevant to the chosen specialization/branch.
13.	**Professional Elective (PE)**	Courses include the elective courses relevant to the chosen specialization/ branch.
14.	**Project Work (PW)**	Refers to the project done by a student or a group of students during final year.
15.	**Career Enhancement Courses (CEC)**	Includes Mini Project Work and / or Internship, Seminar, Professional Practices, Case Study, soft skills and Industrial / Practical Trainings etc.,
16.	**Academic Evaluation Committee (AEC)**	The committee includes Principal, CoE, HoD concerned (For details refer **Appendix V**)
17.	**Department Evaluation Committee (DEC)**	The committee included HoD (need basis), senior faculty member(s) of department from various levels, class advisor, Mentor of the students. (For details refer **Appendix V**)

4. ADMISSION

4.1 Candidates seeking admission to M.E. / M.B.A / M.C.A., Degree Programme :

Candidates for admission to the first semester of the Post-Graduate Degree Programme shall be required to have passed an appropriate Under-Graduate Degree Examination of Anna University or equivalent as specified under qualification for admission as per the Tamil Nadu Common Admission (TANCA) criteria.

Candidates for admission to the III semester of the M.C.A Degree Programme shall be required to have passed an appropriate Under-Graduate Degree Examination of Anna University or equivalent as specified under qualification for admission as per the Government of Tamil Nadu.

Note : TANCA releases the updated criteria during the admissions every academic year.

Admission shall be offered only to the candidates who possess the qualification prescribed against each programme.

Any other relevant qualification which is not prescribed against each programme shall be considered for equivalence by the committee constituted for the purpose. Admission to such degrees shall be offered only after obtaining equivalence to such degrees.

4.2 Re - admission

Students, who have discontinued for reasons other than disciplinary action, may be readmitted as per guidelines given by DoTE, Government of Tamilnadu and Anna University. Department Evaluation Committee (DEC) shall study and recommend on the exception and addition of courses to be registered for, by the student concerned during re-admission. The details shall be forward to Academic Evaluation Committee (AEC) for approval and the committee's decision shall be final.

5. PROGRAMMES OFFERED

KIT offers 2 year (4 Semesters) M.E.. / M.B.A., and 3 year (6 Semesters) M.C.A., Degree programme affiliated to Anna University, under Choice Based Credit System (CBCS) for students admitted from 2019 onwards in the following branches of Engineering and Technology as in Table 1.

Table 1. List of M.E. / M.B.A / M.C.A., programmes offered

M.E., Applied Electronics
M.E., VLSI Design
M.E., Engineering Design
M.E., Computer Science and Engineering
M.E., Power Systems and Engineering
M.B.A., Master of Business Administration
M.C.A., Master of Computer Application

6. ACADEMIC STRUCTURE OF PROGRAMMES

6.1 Medium of Instruction

The medium of instruction is English for all courses, examinations, seminar presentations and project / thesis / dissertation.

6.2 Categorization of Courses

Every Post Graduate Degree Programme will have a curriculum with syllabi consisting of theory and practical courses that shall be categorized as follows :

i. **Foundation Courses (FC)** may include Mathematics or other basic courses

ii. **Professional Core (PC)** courses include the core courses relevant to the chosen specialization/branch.

iii. **Professional Elective (PE)** courses include the elective courses relevant to the chosen specialization/ branch.

iv. **Project Work (PW)** includes Project Work to be done in final semester

v. **Carrear Enhancement Courses (CEC)** includes Mini Project Work and/or Internship, Seminar, Professional Practices, Summer Project, Case Study and Industrial / Practical Training.

Instead of two electives in the curriculum, the student may be permitted to choose a maximum of 2 courses from other PG programmes with the approval of the Head of the Department offering such courses.

6.3 Number of courses per semester

Curriculum of a semester shall normally have a blend of lecture courses and practical courses including Career Enhancement Courses. Each course may have credits assigned as per clause 6.4.

6.4 Credit Assignment

Each course offered is given a T-P-TU-C structure, depending on the number of lecture periods (T), number of periods for practical (P) and number of tutorial periods (T) required per week for an efficient teaching – learning process. A student is expected to put-in his/her own efforts in proportion with periods spent in classroom, as defined in T-P-TU-C structure. On successful completion of the course a student is said to have earned a specified number of credits defined for each course. Each course is assigned certain number of credits based on the following table :

Table 4 : Credit Assigned

Contact period per week	Credits
1 Lecture Period (**T** = Lectures given during class by the faculty)	1
1 Tutorial Periods (**TU =** Tutorial, also class based with more emphasis on problem solving)	1
2 Practical Period (**P**) (Laboratory Periods / CEC / Projects)	1

6.5 Career Enhancement Courses

6.5.1 Industrial Training / Internship

Students shall undergo industrial training/Internship if mandated in the curriculum for periods as specified in the curriculum during the summer/winter vacation, the training being taken on a continuous basis for the periods mentioned. The industry/organization is to be selected with the approval of the Department Evaluation Committee (DEC). Industrial training may also be referred to as “In-plant training”.

The Industrial Training / Internship shall carry 100 marks and shall be evaluated through CIA only. The credit will be awarded to the student after the submission of Internship/Training report to the HoD. The report will be evaluated by a team of (DEC) faculty members nominated by the HoD for awarding the Credit. Based on the recommendation by the team, the student will be awarded credits and the results will be sent to the Controller of Examinations. The awarded credit will taken for CGPA calculation. The final year project period at industry/research organization will not be considered as industrial Training/internship.

6.5.2 Industrial Visit

Every student is required to go for at least one Industrial Visit every year starting from the second year of the Programme subject to the approval of the Head of the Department and Principal. The Heads of Departments shall ensure that necessary arrangements are made in this regard.

6.5.3 Professional Certificate Courses

Students have to undergo one credit courses offered by experts from industry / research organizations and approved by academic council. Students can register such courses from his/her second year of study as and when these courses are conducted by the departments. A student is also permitted to register for these courses of other departments.

If a student does not successfully complete the registered industry supported one credit courses in a semester, the registration of that course will be considered as cancelled. Further, it will not be treated as arrear and if he/she wishes, he/she can re-register for the same course in the ensuing semesters and successfully complete it as and when it is offered subsequently.

6.5.4 Online Courses

Students may be permitted to register for online courses (which are provided with certificate after evaluation of the performance, SWAYAM/NPTEL), during third to sixth semester of his/her study. On successful completion of the course, he/she has to submit the copy of the certificates to the Head of the Department. The assemment will not be calculated for CGPA.

6.5.5 Soft Skills

Every Student is required to go for two soft skill courses during first year of study. The soft skill course includes the communication skill, interpersonal skill and career

development courses. One credit will be awarded for each soft skills courses and it will be included for SGPA/CGPA calculations.

6.5.6 Career Ability Course

The career Ability courses will be designed by the respective department with approval from DEC/AEC based on the industry requirements. One credit will be awarded for each soft skills courses and it will be included for SGPA/CGPA calculations.

6.5.7 Evaluation of One Credit Courses

Students can register for one credit courses in any semester when it is offered. Experts from the industry/Institution (KIT) may design such specialized one-credit courses based on the current technical skill requirements. The Department Evaluation Committee (DEC) shall review and approve the syllabus, course plan, and pedagogy and assessment pattern for the course. One credit courses can also be offered by internal experts i.e faculty members from other departments (not belonging to the specific discipline of the programme) also can offer such courses to the students with the approval of DEC.

A one - credit course shall carry 100 marks and shall be evaluated through Continuous Internal Assessment (CIA) only. The QP pattern and scheme will be decided by the course faculty and will be approved by the DEC/AEC.

The Head of the Department may identify a faculty member as the coordinator for the course. A committee consisting of the Head of the Department, faculty handling the course (if available), coordinator and a senior Faculty member nominated by the Head of the Department shall monitor the evaluation process.

The grades shall be assigned to the students by the above committee based on their performance and included in the calculation of CGPA.

6.5.8 Industry Supported Project Work

The students satisfying the following conditions shall be permitted to carry out their final semester Project work for six months in industry/research organization.

The student should not have current arrears and shall have CGPA of 8.0 and above until 2nd semester (for MBA / ME Students), 4th semester (for MCA students) The student shall undergo the final semester courses in the Pre semester. The Head of Department, in consultation with the faculty handling the said courses shall forward the proposal recommended by the Principal to CoE after approval from AEC at least four weeks before the commencement of the pre - semester of the programme.

6.6 Course Numbering Scheme

Each course is denoted by a unique code consisting of 9 alphanumeric characters. The details of the numbering scheme are in **ANNEXURE - I**.

6.7 Credit Requirement for Programmes

The total number of credits that a student earns during the period of study is called the Total credits. The minimum prescribed credits required for the award of the degree shall be within the limits specified below :

Programme	KIT Credit Range
M.E. / M.Tech.	66-72

Programme	KIT Credit Range
M.B.A.	102
M.C.A. (Regular)	120
M.C.A. (Lateral)	77

7. DURATION OF THE PROGRAMMES

7.1 The minimum and maximum period for completion of the P.G. Programmes are given below :

Programme	Min. No. of Semesters	Max. No. of Semesters
M.E. / M.Tech. (Full-Time)	4	8
M.B.A. (Full Time)	4	8
M.C.A. (Full Time)	6	12
M.C.A.(Lateral)	4	8

7.2 The Curriculum and Syllabi of all the P.G. Programmes shall be approved by the Academic Council of KIT. The number of Credits to be earned for the successful completion of the programme shall be as specified in the Curriculum of the respective specialization of the P.G. Programme.

7.3 Each semester normally consists of 90 working days, including test and examination days. In any contingent situation, the number of working days per semester shall not be less than 65 days. The Principal is given the discretionary powers to decide the number of working days. In such contingencies, the Principal shall ensure that every faculty member teaches the full content of the specified syllabus for the course being taught.

7.3.1 Due to Pandemic / Abnormal situations the Scheme of Examinations and Evaluation will be followed as per the guidelines issued by the Government of Tamil Nadu and Anna University, Chennai.

7.4 The total period for completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not exceed the maximum period specified in clause 7.1 irrespective of the period of break of study in order that he/she may be eligible for the award of the degree.

7.5 For the purpose of regulations, the academic year will be divided into two semesters, the odd semester normally spanning from June to November and the even semester from December to May.

8. COURSE REGISTRATION

Each student, on admission shall be assigned to a mentor who shall advice and counsel the student about the details of the academic programme and choice of courses, considering the student's academic background and career objectives. Some courses require students to register through a course registration process via online.

8.1. Course Registration

Each student on admission shall register for all the courses prescribed in the curriculum in the students first semester of the study.

The registration process for the courses offered in the online registration mode in the forthcoming semester, will commence preferably 10 working days prior to the last working day of the current semester.

A department shall offer a course only if a minimum number of students register for that course. This minimum number may vary from course to course and shall be specified by the department from time to time.

After registering for a course, a student shall attend the classes, satisfy the attendance requirements, earn Continous Assessment Marks and appear for the End Semester Examination (ESE).

8.2 Credits details for Course Registration

Each student has to register for all courses to be undergone in the curriculum of a particular semester (with the facility to drop courses to a maximum of 6 credits). The student can also register for courses for which the student has failed in the earlier semesters.

The registration details of the candidates may be approved by the Head of the Institution and forwarded to the Controller of Examinations. This registration is for undergoing the course as well as for writing the End Semester Examinations.

The courses that a student registers in a particular semester may include

- Courses of the current semester.
- The core (Theory / Lab / CEC) courses that the student has not cleared in the previous semesters.
- Elective courses which the student failed (either the same elective or a different elective instead)

8.3 Flexibility to Drop courses

A student has to earn the total number of credits specified in the curriculum of the respective programme of the study in order to be eligible to obtain the degree. From II semester to Final semesters, the student has the options for dropping an existing course. The total number of credits that a student can drop is limited to 6. Practical courses cannot be dropped.

8.4 Reappearance Registration

8.4.1 If a student fails in a theory or practical course, the student shall do reappearance registration for that course in the subsequent semester by retaining the Continuous Assessment Marks already earned.

8.4.2 If the theory course, in which the student has failed, is a Professional Elective or an Open Elective, the student may register for the same or any other Professional Elective or Open Elective course respectively in the subsequent semesters. Such changes can be done only with due approval by DEC.

8.4.3 The student who fails in Project work/ Seminar other than Practical courses shall register for the same in the subsequent semester and reappear for the End Semester Examination.

8.4.4 If a student is not eligible to appear for end semester examination of a course due to lack of attendance, the student has to register for that course again, when offered next, attend the classes and fulfill the attendance requirements. If the course, in which the student has lack of attendance, is an elective, the student may register for the same or any other elective in the subsequent semesters.

8.4.5 If a student has completed the 8 semesters and has obtained RA grade in one or more courses, he can register and appear for arrear examination directly whenever conducted next.

8.4.6 A student who has already appeared for a course in a semester and passed the examination is not entitled to reappear the same course for improvement of Grade/ Marks.

9. REQUIREMENTS FOR APPEARING FOR CIA, ESE

9.1 A student who has fulfilled the following conditions shall be deemed to be eligible to appear for the CIA-I, CIA-II, CIA-III and ESE. Ideally, every student is expected to attend all the classes and earn 100% attendance. Students who have earned not less than 75% attendance course wise taking into account the number of periods required for that course as specified in the curriculum. Table 5 illustrates the mandatory attendance requirement for CIA-I, CIA-II, CIA-III and ESE.

Table 5 : Mandatory Attendance Requirement for CIA-I, CIA-II, CIA-III and ESE.

Test / Examination Type	Period of Calculation	Minimum % of attendance required
Continuous Internal Assessment Test I (CIA - I)	**First Semester** From the date of joining of course to three working days before the start of CIA - I	60%
	Second to Eighth semester From the date of commencement of the class to one week before the start of CIA - I	75%

Continuous Internal Assessment Test - II (CIA - II)	From the date of joining (1st semester) / date of commencement of class (2nd to 8th Semester) to one week before the start of CIA - II	75% (for students maintaining 80% or more attendance between CIA - I and CIA - II, but falls short of the 75% cumulative requirement, the requirement may be relaxed if recommended by the AEC)
Continuous Internal Assessment Test III (CIA-III)	From the date of joining (1st semester) / date of commencement of class (2nd to 8th Semester) to one week before the start of CIA - III	75% (for students maintaining 80% or more attendance between CIA - II and CIA - III but falls short of the 75% cumulative requirement, the requirement may be relaxed if recommended by the AEC)
End Semester Examination (ESE)	From the date of joining (1st semester) / date of commencement of class (2nd to 8th Semester) to the last day of instruction.	75%

9.1.1 Students having a CGPA of 8.50 and above and with no standing arrears will be exempted from the minimum attendance requirements (from 7th Sem. onwards).

9.1.2 A student shall normally be permitted to appear for End Semester Examination of the course if he / she has satisfied the attendance requirements (vide Clause -9.1). He /she is eligible to register for ESE in that semester by paying the prescribed fee.

9.1.3 A Candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirements for completion of a semester. Ideally every student is expected to attend all classes of all the courses and secure 100% attendance. However, in order to give provision for certain unavoidable reasons such as Medical / participation in sports, the student is expected to attend atleast 75% of the classes. Therefore, he/she shall secure not less than 75%.

9.1.4 However, a candidate who secures overall attendance between 65% and 74% in the current semester due to medical reasons (prolonged hospitalization / accident / specific illness) / Participation in Sports events may be permitted to appear for the current semester examinations subject to the condition that the candidate shall submit the medical certificate / sports participation certificate attested by the Head of the Institution. The same shall be forwarded to the Controller of Examinations for record purposes.

9.1.5 Candidates who secure less than 65% overall attendance and candidates who do not satisfy the clause 9.1.3 and 9.1.4 shall not be permitted to write the semester examination at the end of the semester and not permitted to move to the next semester. They are required to repeat the incomplete semester in the next academic year, as per the norms prescribed.

9.1.6 The students who are consistently good in academics ONLY be considered for the grant of ODL under Co-curricular activities by the competent authorities. The following activities shall be considered for the sanction of ODL;

- **Sports and Games :** TIES, Inter Collegiate, Inter Zonal, Inter University, State Level, National Level and Open Tournaments.
- **NCC :** Camps and expeditions, NSS camps
- Cultural Programme at State, National and International Level
- **Seminar / Symposia :** Paper presentation/Quiz
- Leadership courses organized by other organizations & Alumni Association activities, Association activities, Placement activities.
- Training programs/Internship at industries and Higher learning Institutions
- Personal damage incurred during the extracurricular activities
- The ODL requisition letter shall be forwarded to the Principal through the HoD of the student by the staff-in-charge of the respective activities before completion of every activity.
- The ODL sanctioned letters shall be submitted to the Department Office. The faculty-in-charge of the department office will check the eligibility for the award of attendance at the end of semester and the same may be submitted to DEC for approval.

9.1.7 The student should register all the courses of current semester and all the arrear courses in the previous semesters. If any student fails to register and pay the examination fees within the due date, he / she shall not be permitted to attend the End Semester Examinations. However, he / she will be permitted to continue their studies in the next higher semester, provided that the student satisfies the requirements as stipulated in this clause of this regulation.

9.1.8 Those students who are not deemed to have completed the semester with references to the conditions specified above shall undergo the semester again in all the courses in the respective semester during next academic year. He/she shall seek re-admission as per the norms of the affiliating University / DOTE (Directorate of Technical Education).

The days of suspension for a student on disciplinary grounds will be considered as days of absence for calculating the percentage of attendance for each individual course.

10. PROVISION FOR WITHDRAWAL FROM EXAMINATION

A student may, for valid reasons (medically unfit / unexpected family situations/Sports person representing Tamilnadu / India with prior permission for participation from Principal / CoE / DEC), be granted permission to withdraw (after registering for the examinations) from appearing for any course or courses in the End Semester Examination of a particular semester. The student may withdraw by following the due process of the CoE's office before the commencement of examination. This facility can be availed only once during the entire duration of the degree programme.

Withdrawal from ESE will be valid only if the student is, otherwise, eligible to write the examination and the application for withdrawal is made to the CoE, prior to the examination in the course or courses concerned. The application for withdrawal should be recommended by the Head of the Department concerned and approved by the Head of the Institution.

11. TEMPORARY BREAK OF STUDY FROM A PROGRAMME

11.1 Break of study is normally not permitted. However, if a student intends to temporarily discontinue the programme in the middle of a semester / year for valid reasons (such as Internships, accident or hospitalization due to prolonged ill health) and wishes to re-join the programme in the next academic year, he / she shall apply in advance to the Principal through the Head of the Department, stating the reasons. The application shall be submitted not later than the last date for registering for the semester examinations. Break of study is permitted only once during the entire period of the degree programme.

11.2 The student permitted to re-join the programme after the break shall be governed by the rules and regulations in force, at the time of re-joining.

11.3 The duration specified for passing all the courses for the purpose of classification of degree(vide clause 19) shall be increased by the period of such break of study permitted(vide clause 11)

11.4 If a student is detained for want of requisite attendance, academic progress and good conduct, the period spent in that semester shall not be considered as permitted Break of Study and Clause 11.3 is not applicable for such cases.

12. ASSESSMENT PROCEDURES FOR AWARDING MARKS

The total marks for each course generally (Theory, Practical, Project Work) will be 100, comprising of two components namely Continuous Internal Assessment (CIA) and End Semester Examination (ESE). However, there could be some open elective courses, human excellence courses, one credit industry courses, add-on courses and Mandatory courses that have only continuous assessment for 100 marks without an End Semester Examination. The Department Consultative Committee (DCC) has to approve such courses every semester. The scheme of assessment may also be decided by the faculty handling the course concerned with the approval from DCC and shall be made available to the students during the online course registration. Each course shall be evaluated for a maximum of 100 marks as illustrated in Table 6.

Table 6 : Course Evaluation

S. No.	Category of course	Continuous Internal Assessment	Semester End Examinations
1.	Theory Courses	40 Marks	60 Marks
2.	Laboratory Courses		
3.	Project Work		
4.	Career Enhancement Course (CEC) and Mandatory Course (MC)	100 Marks	–

The End Semester Examination (theory and practical) of 3 hours duration shall ordinarily be conducted between October and December during the odd semesters and between April and June during the even semesters.

The End Semester Examination for project work shall consist of evaluation of the final report submitted by the student or students of the project group (of not exceeding 4 students) by an external examiner and an internal examiner, followed by a viva-voce examination conducted separately for each student by a committee consisting of the external examiner, the supervisor of the project group and an internal examiner.

For the End Semester Examination in both theory and practical courses including project work the internal and external examiners shall be appointed by the Controller of Examinations..

13. MARKS DISTRIBUTION

13.1 Attendance Mark

Marks are awarded for the attendance earned by the students for individual courses as per the following table.

Attendance Range in %	Marks to be earned by the students
96 - 100	5
91 - 95	4
86 - 90	3
81 - 85	2
75 - 80	1

13.2 Question paper pattern

a. Table 7.1 Continuous Internal Assessment

(CIA - I, CIA – II and CIA – III)

2 Marks	12 Marks	Total marks
7	3 (Either or Type)	50

b. Table 7.2 Midsem and Semester End Examinations

2 Marks	13 Marks	15 marks	Total Marks
10	5 (Either or Type)	1 (Either or Type)	100
For Mathematics paper only			
2 Marks	16 Marks		Total Marks
10	5 (Either or Type)		100

13.3 Theory Courses

Continuous Internal Assessment tests are conducted by the Office of the Controller of Examination. Continuous Internal Assessment comprises three Continuous assessment tests, Assignment / Class test / Presentation / Online Test / Mini projects / Tutorials and Attendance. By adopting this method, the students will go through a continuous and systematic study pattern. The Corresponding weightages are given below.

Table 8 : Continuous Internal Assessment Test for Theory Courses

Particulars	Syllabus	Duration	Exam Mark	Internal Mark
Continuous Internal Assessment - I	1.5 Units	1.5 hours	50 marks	10
Continuous Internal Assessment - II	1.5 Units	1.5 hours	50 marks	10
Continuous Internal Assessment - III	1.5 Units	1.5 hours	50 marks	10
Assignment / Class Test / Online Test / Mini Project / Tutorial / Presentation / Online course / Certificate Course				**5**
Attendance				5
Total				**40**

13.4 Criteria for Assessment for Lab Courses

Every exercise / experiment in all practical courses shall be valuated on a continuous basis. The criteria for Continuous Assessment (for each cycle of exercise/experiment) are given in Table 9.

Table 9 : Assessment for Lab Courses

Sl. No.	Description		Weightage
1.	Continuous Internal Assessment Marks (CIAM)		
	a.	Average of Experimental Report / Workbook	25
	b.	Model examination	10
	c.	Attendance	5
	Total CIAM		**40**
2.	Semester End Exam Marks (SEEM)		
	a.	Lab Examination with Viva Voce	60
	Total ESEM		**60**
		Total Marks	**100**

13.5 PROJECT WORK

For Project Work (Phase I & II) out of 100 marks, the maximum marks for Continuous Assessment is 40 marks and that for the End Semester Examination (project report evaluation and viva-voce examination) is 60 marks. Project work may be assigned to a single student or to a group of students not exceeding 4 per group, under the supervision of faculty guide(s).

The Head of the Department shall constitute a review committee for each programme. There shall be a minimum of three faculty members in the review committee. There shall be three reviews (as per **Table 10**) in total, during the semester by a review committee. The student shall make presentation on the progress made before the committee.

Interim project report shall be submitted before the project reviews with the approval of the guide. The Project Report, prepared according to the approved guidelines and duly signed by the guide and the Head of the Department, shall be submitted to the department as per the timeline announced by the department. The End Semester Examination for project work shall consist of evaluation of the final project report by an external examiner, followed by a viva-voce examination conducted separately for each student, by a committee consisting of the external examiner, and an internal examiner. The Controller of Examinations (CoE) shall appoint Internal and External Examiners for the End Semester Examination of the Project Work.

A candidate may, however, in certain cases, be permitted to work on projects in an Industrial/Research Organization, on the recommendations of the Head of the Department Concerned. In such cases, the Project work shall be jointly supervised by a supervisor of the department and an expert, as a joint supervisor from the organization and the student shall be instructed to meet the supervisor periodically and to attend the review committee meetings for evaluating the progress.

The Project work (Phase II in the case of M.E/M.Tech.) shall be pursued for a minimum of 16 weeks during the final semester.

The deadline for submission of final Project Report is 60 calendar days from the last working day of the semester in which project / thesis / dissertation is done. However, the Phase-I of the Project work in the case M.E. / M.Tech. Programmes shall be submitted within a maximum period of 30 calendar days from the last working day of the semester as per the academic calendar published by the University.

The Continuous Internal Marks (CIM) and Semester End marks (SEM) for Project Work and the Viva-Voce Examination will be distributed as indicated in Table 10.

Table 10 : CIM and SEM break-up for project work

<table>
<tr><th>Sl.No.</th><th colspan="2">Review No.</th><th>Description</th><th>Marks</th><th>Total Marks</th></tr>
<tr><td rowspan="7">1.</td><td colspan="5">Continuous Internal Assessment Marks</td></tr>
<tr><td rowspan="2">a.</td><td rowspan="2">Review 1</td><td>Review Committee</td><td>5</td><td rowspan="2">10</td></tr>
<tr><td>Guide</td><td>5</td></tr>
<tr><td rowspan="2">b.</td><td rowspan="2">Review 2</td><td>Review Committee</td><td>7</td><td rowspan="2">15</td></tr>
<tr><td>Guide</td><td>8</td></tr>
<tr><td rowspan="2">c.</td><td rowspan="2">Review 3</td><td>Review Committee</td><td>7</td><td rowspan="2">15</td></tr>
<tr><td>Guide</td><td>8</td></tr>
<tr><td colspan="5">Total CAM</td><td>40</td></tr>
<tr><td rowspan="4">2.</td><td colspan="5">Semester End Examinations Marks</td></tr>
<tr><td rowspan="2">a.</td><td rowspan="2">Evaluation of final report and viva-voce</td><td>Internal Examiner</td><td>10</td><td rowspan="2">50</td></tr>
<tr><td>External Examiner</td><td>40</td></tr>
<tr><td>b.</td><td>Outcome*</td><td>Publication of papers / prototype / patents etc.,</td><td>10</td><td>10</td></tr>
<tr><td colspan="5">Total ESEM</td><td>60</td></tr>
<tr><td colspan="5">Total Marks</td><td>100</td></tr>
</table>

Review committee consists of internal faculty members nominated by the Head of the Department. The guide of student being examined shall not be part of the committee.

* Outcome – in terms of paper publication, patents, product development and industry projects shall be awarded by both internal and external examiners, based on the document proofs submitted by the student concerned.

If a student fails to submit project report / does not appear for the ESE /fails in the End Semester Examination (ESE)/ fails in Continuous Internal assessment (CIA) he/she is deemed to have failed in the project work and shall have to re-register for the same when offered next.

14. PASSING REQUIREMENTS

14.1 A student is declared to have successfully passed a theory based course if he / she has secured:

- A minimum of 50% marks in the End Semester Examinations.
- A minimum of 50% marks on combining both Continuous Internal Assessment Marks (CIAM) and End Semester Examination Marks (ESEM).

14.2 A student is declared to have successfully passed a practical / project based course if he/she has secured:

- A minimum of 50% marks in the End Semester Examinations.
- A minimum of 50% marks on combining both Continuous Internal Assessment Marks (CIAM) and End Semester Examination Marks (ESEM).

14.3 For a student who does not meet the minimum passing requirements, the term "RA" against the course will be indicated in his/her grade sheet. He/she shall reappear in the subsequent examinations for the course as arrear or re-register for the course when offered .

14.4 For a student who is absent for end-semester theory / practical / project viva-voce, the term "RA" will be indicated against the corresponding course. He/she shall reappear for the End Semester Examination of that course as arrear in the subsequent semester or when offered next.

14.5 The letter grade "W" will be indicated for the courses for which the student has been granted authorized withdrawal (refer Clause 10).

14.6 For mandatory courses (non-credit), the student must satisfy the minimum attendance requirement & passing criteria as specified for the course as detailed in Section 16.2

15. METHODS FOR REDRESSAL OF GRIEVANCES IN EVALUATION

Students who are not satisfied with the grades awarded in the End Semester Examination of Theory for regular and arrear exams can seek redressal as illustrated in Table 11.

Table 11: Grievance Redressal Mechanism

Sl. No.	Redressal Sought	Methodology	
		Regular Exam	Arrear Exam
1.	Revaluation	Apply for photo copy of answer book Then apply for revaluation after course expert recommendation	
2.	Challenge of Evaluation	Apply for photo copy of answer book Then apply for revaluation after course expert recommendation Next apply for challenge of evaluation	
Note : All applications to be made to COE along with the payment of the prescribed fee.			

Challenge of Evaluation – Flow Process

Table 12 : Evaluation – Flow Process

Step 1	A student can make an appeal to the CoE for the review of answer scripts after paying the prescribed fee.
Step 2	CoE will issue the photocopy of answer scripts to the student.
Step 3	The faculty who had handled the subject will evaluate the script and HoD will recommend.
Step 4	A committee consisting of 2 evaluators appointed by CoE will review and declare the result.
Step 5	If the result is in favour of the student, the fee collected will be refunded to the student.
Step 6	The final mark will be announced by CoE.

16. LETTER GRADE

Absolute grading system is adopted in converting marks to grads.

16.1 Absolute Grading Policy

All assessments of a course will be evaluated on absolute marks basis. However, for the purpose of reporting the performance of a candidate, letter grades, each carrying certain number of points, will be awarded as per the range of total marks (out of 100) obtained by the candidate in each subject as detailed below :

Table 13: Absolute Grading – Letter Grade and its Range

Sl.No.	Range of percentage of total marks	Letter Grade	Grade Points
1.	91 - 100	O (Outstanding)	10
2.	81 – 90	A+ (Excellent)	9
3.	71 – 80	A (Very Good)	8
4.	61 – 70	B+ (Good)	7
5.	50 – 60	B (Average)	6
6.	<50	RA (Re-appearance)	0
7.	Shortage of attendance	RA - SA (Re-appearance due to shortage of attendance)	0
8.	Absent	RA – AB (Re-appearance due to absence)	0

9.	Withdrawal from examination	W	0
10.	Pass in Mandatory non-credit courses	P	0
11.	Fail in Mandatory non-credit courses	F	0

A student is deemed to have passed and acquired the corresponding credits in a particular course if he/she obtains any one of the following grades: "O", "A+", "A", "B+","B". 'RA' indicates that Reappearance is mandatory for that course concerned. 'SA' denotes shortage of attendance (as per Clause 9) and hence prevented from writing the End Semester Examination. P and F are grades for mandatory, but non-credit courses.

16.2 Grading for Mandatory Courses

Mandatory Courses are courses that are required to be completed to fulfill the degree requirements (e.g. Human excellence, Environmental science, etc.). They are normally non – credit based. These courses will not be taken in to consideration for the SGPA / CGPA calculations. Each of these courses is assessed continuously and internally for a total mark of 100. The pass mark is 50%. Students, who fail to pass this course, are required to repeat the course, when offered next.

16.2.1 For Mandatory non-credit courses the student must satisfy the minimum attendance requirement & passing criteria as specified for the course. These courses do not carry credits but needs to be completed to fulfill the degree requirements.

16.2.2 For the Mandatory non-credit courses student completing the course will be awarded Pass grade (P) and those who fail to satisfy the attendance requirement or fail to satisfy the minimum passing requirement of 50% marks, will be awarded Fail (F) grade and the student must re-register for the course when it is offered next.

16.3 Formula for SGPA and CGPA calculations

After the results are declared, grade sheets will be issued to each student, which will contain the following details :

- The College Name and Affiliating University.
- The list of courses registered during the semester and the grades scored.
- The Semester Grade Point Average (SGPA) for the semester.
- The Cumulative Grade Point Average (CGPA) of all courses enrolled from first semester onwards.

On completion of a semester, each student is assigned a Semester Grade Point Average which is computed as below for all courses registered for, by the student during that semester.

$$\textbf{S}\text{emester }\textbf{G}\text{rade }\textbf{P}\text{oint }\textbf{A}\text{verage} = \frac{\sum(C_i \times GP_i)}{\sum C_i}$$

where C_i is the credit for a course in that semester and GP_i is the Grade Point earned by the student for that course. The **SGPA** is rounded off to two decimals.

The overall performance of a student at any stage of the Degree programme is evaluated by the **C**umulative **G**rade **P**oint **A**verage **(CGPA)** up to that point of time

$$\textbf{C}\text{umulative }\textbf{G}\text{rade }\textbf{P}\text{oint }\textbf{A}\text{verage} = \frac{\sum(C_i \times GP_i)}{\sum C_i}$$

where C_i is the credit for each course in each of the completed semesters at that stage and GP_i is the grade point earned by the student for that course. The **CGPA** is rounded off to two decimals.

16.4 Formula for Calculating Percentage

CGPA x 10 = % of Marks

17. ELIGIBILITY FOR THE AWARD OF DEGREE

A student shall be declared to be eligible for the award of the B.E. / B.Tech. Degree provided the student has

i. Successfully gained the required number of total credits as specified in the curriculum corresponding to the student's programme within the stipulated time.

ii. Successfully completed the course requirements, appeared for the End Semester examinations and passed all the subjects prescribed in clause no.7.

iii. Successfully passed any additional courses prescribed by the Academic council

iv. Successfully passed any additional courses prescribed by the Department & concerned whenever readmitted under regulations 2019. (R19) (vide Clause 4.2)

v. No disciplinary action pending against the student.

vi. The award of Degree must have been approved by the Academic Council of KIT.

18. CLASSIFICATION OF M.E / MBA / MCA DEGREE

The degree awarded to eligible students will be classified as given in Table 14.

Table 14: Classification of the ME/MBA/MCA Degree

Sl.No.	Class Awarded	Criteria
1.	First class with distinction	A student who satisfies the following conditions shall be declared to have passed the examination in First class with Distinction : **M.E. / M.B.A.** › Should have passed the examination in all the courses of all the four semesters in the student's First Appearance within **three** years, which includes authorised break of study of one year (if availed). Withdrawal from examination will not be considered as an appearance. › Should have secured a CGPA of not less than **8.50**. › Should NOT have been prevented from writing end Semester examination due to lack of attendance in any of the courses.

		M.C.A › Should have passed the examination in all the courses of all the six semesters in the student's First Appearance within four years, which includes authorised break of study of one year (if availed). Withdrawal from examination will not be considered as an appearance. › Should have secured a CGPA of not less than **8.50**. › Should NOT have been prevented from writing end Semester examination due to lack of attendance in any of the courses.
2.	First Class	A student who satisfies the following conditions shall be declared to have passed the examination in **First class** : **M.E. / M.Tech. / M.B.A.** › Should have passed the examination in all the courses of all four semesters **within three years**, which includes one year of authorized break of study (if availed) or prevention from writing the End Semester Examination due to lack of attendance (if applicable). › Should have secured a CGPA of not less than **7.00**. **M.C.A** › Should have passed the examination in all the courses of all six semesters **within four years**, which includes one year of authorized break of study (if availed) or prevention from writing the End Semester Examination due to lack of attendance (if applicable). › Should have secured a CGPA of not less than **7.00**.
3.	Second Class	All other students (not covered in clauses Sl.No.1 and 2 under clause 19) who qualify for the award of the degree (vide Clause 20) shall be declared to have passed the examination in Second Class.
Note : A student who is absent for the End Semester Examination in a course / project work Viva Voce after having registered for the same will be considered to have appeared for that examination (except approved withdrawal from End Semester Examinations as per Clause 9) for the purpose of classification.		

19. AWARD OF DEGREE

The Academic Council of the institution will approve the award of Degree to all eligible students. The degree will be issued by Anna University, Chennai and the consolidated Grade Sheet will be issued by the institution. The consolidated grade sheet will specify any specializations and distinctions that the student has earned during the course of the study.

20. FACULTY MENTOR

To help the students in palnning their courses of study and for general advice on the academic progarmme, the Head of the Department will attach a certain number of students (maximum 20) to a faculty member of the department. He/She shall function as Faculty Mentor for these students throughout their period of study. The faculty mentor shall,

- Advice the students in registering and reappearance registering of courses
- Monitor their attendance, academic progress and discipline of the students
- Counsel periodically or during the faculty mentor meeting scheduled in the class time table.
- Inform the students about the various facilities and activities available to enhance the student's curricular and co-curricular activities.
- If necessary, the faculty mentor may also discuss with or inform the parents about the progress of the students through Head of the Department or in Parent-Teacher meeting.

21. CLASS COMMITTEE

The objective of the Class Committee is to improve the teaching-learning process.

The functions of the class committee include :

- Resolving difficulties experienced by students in the classroom and in the laboratories.
- Clarifying the regulations of the degree programme and the details of rules therein.
- Discussing the progress of academic schedule and deviations if any.
- Evaluating the performance of the students of the class after each test and finding the ways and means of improvement.
- Every class in first year of study shall have a class committee consisting of faculty members who are teaching in that class, student representatives (cross section of students from boys and girls) and a chairperson who is a faculty not handling the course for the class.
- From III semester onwards, Class committee comprises of all the faculty members who are handling courses in that particular semester and two student representatives from each course. A chairperson who is a faculty not handling course for that particular semester, nominated by the Head of the Department shall coordinate the activities of this committee.
- The class committee shall be constituted by the Head of the Department/Chief Tutor on the first week of commencement of the semester.
- The class committee shall meet three times in a semester as specified in the academic calendar.
- The Principal may participate in any class committee of the institution.
- During these meetings, the representative of the class shall meaningfully interact and express the opinions and suggestions of the other students of the class to improve the effectiveness of the teaching-learning process.
- The Chairperson is required to prepare the minutes of the meeting, signed by the members and submit the same to Head of the Department within five working days of the meeting. Head of the Department will in turn consolidate and forward the same to the Principal, within 10 working days of the meeting.
- In each meeting, the action taken report of the previous meeting is to be presented by the Chairperson of the class committee.

22. COMMON COURSE COMMITTEE

- A theory course handled by more than one teacher shall have a "Common Course Committee" comprising of all teachers teaching that course and few students who have registered for that course. There shall be two student representatives from each batch of that course. One of the teachers shall be nominated as Course Coordinator by the HoD concerned and duly approved by the Principal
- The first meeting of the Common Course Committee shall be held within fifteen days from the date of commencement of the semester. The nature and weightage of the continuous assessments shall be decided in the first meeting, within the framework of the Regulations. Two or three subsequent meetings in a semester may be held at suitable intervals. During these meetings, the student members shall meaningfully interact and express their opinions and suggestions of all the students to improve the effectiveness of the teaching-learning process. It is the responsibility of the student representatives to convey the proceedings of these meetings to the whole batch.
- In addition, the "Common Course Committee" (without the student representatives) shall meet to ensure uniform evaluation of continuous assessments after arriving at a common scheme of evaluation for the assessments.
- Wherever feasible, the common course committee (without the student representatives) shall also prepare a common question paper for the continuous assessment tests. The question paper for the end semester examination is common and shall be set by the Course Coordinator in consultation with all the teachers or the external member as appointed by the Controller of Examinations.

23. DETAILS OF FACULTY PEDAGOGICAL AND STUDENT ASSESSMENT RECORD

Every teacher is required to maintain a Faculty Record Book/ course file consisting of the following details as shown below;

- Time-table, course syllabus, program outcomes, course outcomes.
- Details of attendance of each student marked in each theory/practical/project work class.
- CIA marks, Midsem marks, Details of Assignment/ seminar given, course delivery details, corrective and preventive actions on test performance of students and any other additional details.

The record book should be submitted to the HOD periodically (at least three times in a semester) for checking the syllabus covered, the test marks and attendance. The HOD shall put his/her signature and date in the record book after due verification. At the end of the semester, the record book shall be verified by the Principal who will also ensure safe custody of the document for at least four years. The university or any inspection team appointed by the University / UGC / AICTE may verify the records of attendance and assessment of both current and previous semesters.

24. DISCIPLINE

Every student is required to maintain discipline and decorum both inside and outside the institution campus. They shall follow all the rules and regulations and should not indulge in any

activity which can tarnish the reputation of the University or Institution. The Principal shall refer any act of indiscipline by students to the Discipline and Welfare Committee and other appropriate committees for action.

25. REVISION OF REGULATIONS AND CURRICULUM

The institution may from time to time revise, amend or change the Regulations, scheme of Examinations and syllabi, if found necessary. Academic Council assisted by Board of Studies and Standing Committee will make such revisions / changes.

Note : Any ambiguity in interpretation of this regulation is to be put up to the Standing Committee, whose decision will be final.

26. SPECIAL CASES

In the event of any clarification in the interpretation of the above rules and relations, they shall be referred to the Standing Committee. The standing committee will offer suitable interpretations/ clarifications/amendments required for special case on such references and get them ratified in the next meeting of the Academic Council. The decision of the Academic Council is final.

ANNEXURE - I

COURSE NUMBERING SCHEME

M	1	9	M	E	T	7	0	9
Programme	Regulation		Department Code		Course Type	Semester	Sequence Number	

Programme :
Masters Degree (M.E. / M.Tech / MBA / MCA) - M

Regulation :
R – 19

Department Code
AE - Applied Electronics
CS - Computer Science and Engineering
ED - Engineering Design
PS - Power System Engineering
VD - VLSI Design
CA - Computer Application
MB - Management Studies
EN - English
MA - Mathematics
CE - Career Enhancement
MC - Mandatory Course

Course Type
T - Theory
P - Practical / Project/ Internship
E - Elective
O - Open Elective
C - One Credit Courses
N - Online courses
S - Special Electives

Semester
1 - First Semester
2 - Second Semester
3 - Third Semester
4 - Fourth Semester
5 - Fifth Semester
6 - Sixth Semester

Sequence Number
00-99

ANNEXURE - II

POLICY ON MALPRACTICES

GENERAL

- It shall be the endeavour of all concerned to prevent, control and take remedial action to bring about the occurrences of malpractices to “Zero” in Examinations (both Internal and External), Assignments and in all Academic class works.
- Therefore, a comprehensive approach to the malady of malpractices has to be adopted to create a mindset of integrity and honesty, and at the same time take sufficiently stern action to make it clear that such attempts are fraught with comparably very high risk.
- In keeping with this stance, the following measures are to be taken by all concerned from class room level to the Examination Halls:

A. PREVENTION (This is the best method of tackling this malady)

a. Class room level :

All faculty members are to involve themselves in a psychological growth of students by personal example and self-respect and strive towards

- Developing a sense of honour in the minds of students so that they look down upon earning undeserved marks.
- Imbibing a sense of self-respect and internal dignity that prevents him/her from succumbing to the temptation of easy marks by cheating.
- Generating an awareness of the risks to their character and career if convicted, while also explaining the process and strict rules and regulations adopted by the educational system to prevent malpractices.
- Taking stern view of copied assignments and attempts at malpractices in internal examinations also merits equal seriousness as external examinations.
- Setting sufficiently strong deterrent rules in place and regulations like intimation to parents and warning to students in the presence of parents etc. even in case of efforts at malpractices in internal tests and/or repeated acts despite warnings in case of assignments also.

Examination Halls :

Detailed instructions on Invigilation, question paper setting and evaluation and such other instructions will be issued for Invigilation, vigilance, which are to be brought to the notice of all students prior to the examinations.

B. PENAL ACTION FOR MALPRACTICES

All instances of malpractices will be forwarded to the Principal / Chief Superintendents. The offences will be investigated by a Standing Enquiry Committee constituted by Principal, The committee is to summon and give the student an opportunity to present / plead his/her case. The Committee may also summon anybody else, if it so deems necessary for the conduct of enquiry, in the interest of proper investigation and dispensation of the case. The tenure of the committee would be a complete Academic year.

The Committee is to be guided by the following :

- The seriousness of the malpractice, in terms of deviousness, and culpability / criminality of motive.
- The seriousness in terms of effort and degree of deviousness and culpability / criminality of effort.
- Any FIR / Police case that has been registered in the first instance by the Principal / Chief Superintendent.
- Any other special consideration either mitigating or to the contrary.

C. PENALTY FOR OFFENSES

The penalties awarded will depend on the seriousness of the Offence. A list of Offences and penalties are placed at Annexure III.

The Enquiry Report with findings and recommendations of the Committee are to be forwarded to the Controller who will undertake necessary follow up action. Based on the recommendations of the Controller of Examinations, the Principal is empowered to award penalties for offences classified as belonging to categories 1 to 7 of the offence table. The cases falling in categories from S.No. 8 onwards are to be put up to the Principal for consideration and award of suitable penalty.

ANNEXURE - III

Sl.No.	Nature of Malpractice	Maximum Punishment
1.	Appeal by the candidate in the answer script to show mercy by way of awarding more than deserving marks.	Fine of Rs. 1000/- per subject.
2.	The candidate writing his/her name in the answer script.	
3.	The candidate writing his/her registration number/college name in places other than specified in the answer script	
4.	Any special marking in the answer script by the candidate.	
5.	The candidate communicating with neighbouring candidate orally or non-verbally; the candidate causing suspicious movement of his/her body.	
6.	Irrelevant writing by the candidate in the answer script.	
7.	The candidate writing answer on his/her question paper or making use of his/her question paper for rough work	

8.	The candidate possessing cell phones / programmable calculator(s) / any other electronic storage device(s) gadgets	Invalidating the examination of the particular subject written by the candidate
9.	The candidate possessing cell phones / programmable calculator(s) / any other electronic storage device(s) **gadgets**	Invalidating the examination of the particular subject written by the candidate
10.	The candidate possessing any incriminating material(s) (whether used or not). For example:-Written or printed materials, bits of papers containing written information, writings on scale, calculator, handkerchief, dress, part of the body, Hall Ticket, etc.	Invalidating the examination of the subject concerned and all the theory and the practical subjects of the current semester registered by the candidate. Further the candidate is not considered for revaluation of answer scripts of the arrears-subjects. If the candidate has registered for arrears – subjects only, invalidating the examinations of all the arrears – subjects registered by the candidate.
11.	The candidate possessing cell phone(s)/ programmable calculator(s)/any other electronic storage device(s) gadgets and containing incriminating materials (whether used or not).	
12.	The Candidate possessing the question paper of another candidate with additional writing on it.	
13.	The candidate passing his/her question paper to another candidate with additional writing on it	
14.	The candidate passing incriminating materials brought into the examination hall in any medium (hard/soft) to other candidate(s).	
15.	The candidate copying from neighbouring candidate.	
16.	The candidate taking out of the examination hall answer booklet(s), used or unused	
17.	Appeal by the candidate in the answer script coupled with a promise of any form of consideration.	
18.	Candidate destroying evidence relating to an alleged irregularity.	Invalidating the examinations of the subject concerned and all the theory and the practical subjects of the current semester registered by the candidate.

		Further the candidate is not considered for revaluation of answer scripts of the arrears-subjects. If the candidate has registered for arrears – subjects only, invalidating the examinations of all the arrears – subjects registered by the candidate. **Additional Punishment :** i. i. If the candidate has not completed the programme, he/she is debarred from continuing his/her studies for one year i.e., for two subsequent semesters. However the student is permitted to appear for the examination in all the arrears-subjects during the debarred period. ii. If the candidate has completed the programme, he/she is prevented from writing the examinations of the arrears-subjects for two subsequent semesters..
19.	Vulgar/offensive writings by the candidate in the answer script.	Invalidating the examinations of all the theory and practical subjects of the current semester and all the arrears –subjects registered by the candidate.
20.	The candidate possessing the answer script of another candidate	
21.	The candidate passing his /her answer script to another candidate	
22.	Involved in any one or more of the malpractices of serial no. 8 to 21 for the second or subsequent times.	Invalidating the examinations of all the theory and practical subjects of the current semester and all the arrears –subjects registered by the candidate. **Additional Punishment :** i. If the candidate has not completed the programme, he/she is debarred from continuing his/her studies for one year i.e., for two subsequent semesters. However the student is permitted to appear for the examination in all the arrears-subjects during the debarred period. ii. If the candidate has completed the programme, he/she is prevented from writing the examinations of the arrears-subjects for two subsequent semesters.
23.	The candidate substituting an answer book let prepared outside the examination hall for the one already distributed to the candidate	

24.	The candidate indulge in any disruptive conduct including, but not limited to, shouting, assault of invigilator, officials or students using abusive and /or threatening language, destruction of property.	Invalidating the examinations of all the theory and practical subjects of the current semester and all the arrears –subjects registered by the candidate. **Additional Punishment :** i. If the candidate has not completed the programme, he/she is debarred from continuing his/her studies for two years i.e., for four subsequent semesters. However the student is permitted to appear for the examination in all the arrears-subjects during the debarred period. ii. If the candidate has completed the programme, he/she is prevented from writing the examinations of the arrears -subjects for four subsequent semesters.
25.	The candidate harass or engage others to harass on his/her behalf an invigilator, official, witnesses or any other person in relation to an irregularity by making telephone calls, visits, mails or by any other means.	
26.	Candidate possessing any firearm/weapon inside the examination hall.	
27.	Cases of Impersonation	i. Handing over the impersonator to the police with a complaint to take appropriate action against the person involved in the impersonation by the Chief Supt. If a student of this University is found to impersonate a 'bonafide student', the impersonating student is debarred from continuing his/her studies and writing the examinations **permanently**. He/she is not eligible for any further admission to any programme of the University. Debarring the 'bonafide student' for whom the impersonation was done from continuing his/her studies and writing the examinations **permanently**. He/she is not eligible for any further admission to any programme of the University.

ANNEXURE - IV

Process to Consider the Application for Revocation of Detainment

The process to consider the application for revocation of detainment on account of lack of attendance in 3 or more courses, due to genuine reasons (viz. sports participation, NCC, Medical Grounds etc.) is as follows :

The student submits an application for consideration via a request letter to the CoE,not later than 3 days from the last working day, along with the HoD's recommendation, Class Advisor's report and Mentor's recommendation. A committee consisting of the Principal, CoE, HoD (Respective Department) and HoD's-2 from departments other than the student's own. The committee shall meet within 4 working days,to consider the case. Stakeholders may be called to be present in the meeting as may be required, and Decision arrived at. The decision approved by Principal shall be final.

ANNEXURE - V

Academic Evaluation Committee (AEC)

The committee includes the Principal, CoE, HoD concerned. The committee meets to carry out business related to academic matters which require central decision making and approval viz. retest approval of missed CIA, addressing the feedback collected from the various departments' class committee meetings.

Department Evaluation Committee (DEC)

The committee includes HoD (need basis), and a few faculty members of the department from various levels. The committee meets to carry out business related to academic matters that can be addressed within the department viz. course equivalence of common courses for readmitted students; approval of new courses to be offered by the department; consider and approve the credit equivalence of courses offered by industry, review the course offerings; consider the merit of applications involving lack of attendance in PE/OE courses to take up another PE or OE; approve CIAM only courses every semester; approve scheme of assessment for each course; Approval for and Mapping credits of certification courses; approval of list of nationally or internationally recognized professional certification courses with prometric testing.

Curriculum

Conceptual Frame work

(For Students admitted from the Academic Year 2019-20 and onwards)

Semester	Level of Course	Hrs. / Week	No. of Courses	Range of Credits / Courses	Total Credits
PART - I					
A - Foundation Courses					
I	Foundation Courses (FC)	4	1	4	4
B - Professional Core Courses					
I to III	Professional Core (PC)	3	11	2 - 3	31
C - Elective Courses					
I to III	Professional Elective (PE)	3	5	3	15
D - Project Work					
III & IV	Project Work (PW)	12 -24	2	6 -12	18
Total Credit					**68**
PART II - Career Enhancement Courses (CEC)					
II	Article Writing and Seminar	2	1	1	1
Total Credit					**01**
Total Credit to be Earned					**69**

BoS Chairman

Scheme of Instructions and Examinations

(For Students admitted from the Academic Year 2019-20 and onwards)

Semester - I

Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19MAT101	Applied Mathematics for Electronics Engineers	FC	4	3	0	1	3	40	60	100	4
M19VDT101	Advanced Digital System Design	PC	3	3	0	0	3	40	60	100	3
M19VDT102	CMOS Digital VLSI Design	PC	3	3	0	0	3	40	60	100	3
M19VDT103	DSP Integrated Circuits	PC	3	3	0	0	3	40	60	100	3
M19VDT104	CAD for VLSI Circuits	PC	3	3	0	0	3	40	60	100	3
M19VDT105	Analog IC Design	PC	3	3	0	0	3	40	60	100	3
M19VDP101	VLSI Design Laboratory - I	PC	4	0	4	0	3	40	60	100	2
Total Contact Hours / Week			23	18	4	1	Total Credits				21

Semester - II

Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDT201	Testing of VLSI Circuits	PC	3	3	0	0	3	40	60	100	3
M19VDT202	VLSI Signal Processing	PC	3	3	0	0	3	40	60	100	3
M19VDT203	Low Power VLSI Design	PC	3	3	0	0	3	40	60	100	3
	Professional Elective - I	PE	3	3	0	0	3	40	60	100	3
	Professional Elective - II	PE	3	3	0	0	3	40	60	100	3
	Professional Elective - III	PE	3	3	0	0	3	40	60	100	3
M19VDP201	VLSI Design Laboratory - II	PC	4	0	4	0	3	40	60	100	2
M19CEP201	Article Writing and Seminar	CEC	2	0	2	0	-	100	-	100	1
Total Contact Hours/Week			24	18	6	0	Total Credits				21

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Semester - III											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDT301	Analog to Digital Interfaces	PC	3	3	0	0	3	40	60	100	3
	Professional Elective - IV	PE	3	3	0	0	3	40	60	100	3
	Professional Elective - V	PE	3	3	0	0	3	40	60	100	3
M19VDP301	Project Work (Phase I)	PW	12	0	12	0	3	40	60	100	6
Total Contact Hours / Week			21	9	12	0	Total Credits				15

Semester - IV											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDP401	Project Work (Phase II)	PW	24	0	24	0	3	40	60	100	12
Total Contact Hours / Week			24	0	24	0	Total Credits				12

FOUNDATION COURSES (FC)											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19MAT101	Applied Mathematics for Electronics Engineers	FC	4	3	0	1	3	40	60	100	4

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PROFESSIONAL CORE (PC)											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDT101	Advanced Digital System Design	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDT102	CMOS Digital VLSI Design	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDT103	DSP Integrated Circuits	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDT104	CAD for VLSI Circuits	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDT105	Analog IC Design	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDP101	VLSI Design Laboratory- I	**PC**	3	3	0	0	**3**	40	60	100	**2**
M19VDT201	Testing of VLSI Circuits	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDT202	VLSI Signal Processing	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDT203	Low Power VLSI Design	**PC**	3	3	0	0	**3**	40	60	100	**3**
M19VDP201	VLSI Design Laboratory-II	**PC**	3	3	0	0	**3**	40	60	100	**2**
M19VDT301	Analog to Digital Interfaces	**PC**	3	3	0	0	**3**	40	60	100	**3**

PROFESSIONAL ELECTIVES (PE)											
Semester – I											
Elective – I											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDE201	Device Modelling	**PE**	3	3	0	0	**3**	40	60	100	**3**
M19AEE101	Computer Architecture and Parallel Processing	**PE**	3	3	0	0	**3**	40	60	100	**3**
M19AET301	Advanced Microprocessors and Microcontrollers Architecture	**PE**	3	3	0	0	**3**	40	60	100	**3**
M19AEE103	Neural Networks and Applications	**PE**	3	3	0	0	**3**	40	60	100	**3**

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Semester - II											
Elective – II											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDE202	ASIC and FPGA Design	PE	3	3	0	0	3	40	60	100	3
M19VDE203	Nano Electronics	PE	3	3	0	0	3	40	60	100	3
M19AEE201	High Performance Networks	PE	3	3	0	0	3	40	60	100	3
M19AEE202	Wireless Adhoc and Sensor Networks	PE	3	3	0	0	3	40	60	100	3

Semester - II											
Elective – III											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDE202	System on Chip Design	PE	3	3	0	0	3	40	60	100	3
M19AET201	Soft Computing and Optimization Techniques	PE	3	3	0	0	3	40	60	100	3
M19VDE205	Reconfigurable Architectures	PE	3	3	0	0	3	40	60	100	3
M19VDE206	Signal Integrity for High Speed Networks	PE	3	3	0	0	3	40	60	100	3

Semester - III											
Elective – IV											
Course Code	Course Name	Category	Instructional Hours				Assessment				Credit
			Contact Periods	T	P	TU	Hours of Exam. (ESE)	CIA	ESE	Total	
M19VDE301	Principles of Remote Sensing	PE	3	3	0	0	3	40	60	100	3
M19AEE303	Advanced Digital Image Processing	PE	3	3	0	0	3	40	60	100	3
M19AEE304	Pattern Recognition	PE	3	3	0	0	3	40	60	100	3
M19AET102	Embedded System Design	PE	3	3	0	0	3	40	60	100	3

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Semester - III											
Elective – V											
Course Code	**Course Name**	**Category**	**Instructional Hours**				**Assessment**				**Credit**
			Contact Periods	**T**	**P**	**TU**	**Hours of Exam. (ESE)**	**CIA**	**ESE**	**Total**	
M19VDE302	MEMS and NEMS	**PE**	3	3	0	0	**3**	40	60	100	**3**
M19VDE303	Hardware-Software Co- Design	**PE**	3	3	0	0	**3**	40	60	100	**3**
M19AEE205	Robotics	**PE**	3	3	0	0	**3**	40	60	100	**3**
M19VDE304	Solid State Device Modelling and Simulation	**PE**	3	3	0	0	**3**	40	60	100	**3**

PROJECT WORK (PW)											
Course Code	**Course Name**	**Category**	**Instructional Hours**				**Assessment**				**Credit**
			Contact Periods	**T**	**P**	**TU**	**Hours of Exam. (ESE)**	**CIA**	**ESE**	**Total**	
M19VDP301	Project Work (Phase I)	**PW**	12	0	12	0	**3**	40	60	100	**6**
M19VDP401	Project Work (Phase II)	**PW**	24	0	24	0	**3**	40	60	100	**12**

CAREER ENHANCEMENT COURSE (CEC)											
Course Code	**Course Name**	**Category**	**Instructional Hours**				**Assessment**				**Credit**
			Contact Periods	**T**	**P**	**TU**	**Hours of Exam. (ESE)**	**CIA**	**ESE**	**Total**	
M19CEP201	Article Writing and Seminar	**CEC**	2	0	2	0	**3**	100	-	100	**1**

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Semester - I

M.E.	M19MAT101 - APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS (Common to VLSI & AE)	T	P	TU	C
		3	0	1	4

Course Objectives	
1.	To demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering.
2.	To extend matrix theory in the field of communication engineering.
3.	To understand the basic concepts of probability and random variables to introduce some standard distributions applicable to engineering which can describe real life phenomenon.
4.	To understand the concept of dynamic programming and apply in communication networks.
5.	To understand the basic concepts of Queueing Models and to apply in real life engineering problems.

UNIT – I	FUZZY LOGIC	12
Classical logic – Multi valued logics - Fuzzy propositions – Fuzzy quantifiers.		

UNIT – II	MATRIX THEORY	12
Cholesky decomposition - Generalized Eigenvectors - Canonical basis- QR factorization - Least squares method - Singular value decomposition.		

UNIT – III	PROBABILITY AND RANDOM VARIABLES	12
Probability - Axioms of probability - Conditional probability - Random variables - Probability function - Moments - Moment generating functions and their properties - Binomial, Poisson, Geometric, Uniform, Exponential and Normal distributions.		

UNIT – IV	DYNAMIC PROGRAMMING	12
Dynamic programming - Principle of optimality - Forward and backward recursion - Applications of dynamic programming: Shortest distance Problem in communication networks - Problems of dimensionality.		

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UNIT – V	LAPLACE TRANSFORMS	12
Existence conditions - Properties (excluding proofs) - Transform of standard functions - Transforms of derivatives and integrals - Periodic function – Inverse Laplace transform - Applications to solution of linear second order ordinary differential equations with constant coefficients		
		Total Instructional hours : 60

Course Outcomes : Students will be able to	
CO1	Make use of Eigen values and Eigen vectors to reduce the quadratic form into canonical form and to find the powers of a square matrix.
CO2	Determine solution for maxima and minima problems.
CO3	Solve differential equations which existing in different engineering disciplines.
CO4	Develop the applications of differential equations in various engineering field.
CO5	Apply Laplace transform and inverse transform to solve differential equations with constant coefficients.

Reference Books	
1.	Bronson, R., “Matrix Operations”, Schaum's Outline Series, (McGraw Hill), 2nd Edition, 2011.
2.	George, J. Klir. and Yuan, B., “Fuzzy sets and Fuzzy logic, Theory and Applications”, (Pearson Education, India) 1st Edition, 2015.
3.	Gross, D., Shortle J.F., Thompson, J.M., and Harris, C. M., “Fundamentals of Queueing Theory”, (John Wiley), 4th Edition, 2014.
4.	Johnson, R.A., Miller, I and Freund J., “Miller and Freund’s Probability and Statistics for Engineers”, (Pearson Education, Asia), 8th Edition, 2015.
5.	Taha, H.A., “Operations Research: An Introduction”, (Pearson education, Asia), New Delhi, 9th Edition, 2016.

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M.E.	M19VDT101- ADVANCED DIGITAL SYSTEM DESIGN (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce methods to analyze and design synchronous sequential circuits.
2.	To introduce methods to analyze and design asynchronous sequential circuits.
3.	To introduce fault diagnosis and testing algorithms.
4.	To introduce the architectures of programmable devices.
5.	To introduce design and implementation of digital circuits using programming tools.

UNIT – I	SEQUENTIAL CIRCUIT DESIGN	9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM.

UNIT – II	ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN	9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit- Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.

UNIT – III	FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS	9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self-test.

UNIT – IV	SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES	9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

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UNIT – V	SYSTEM DESIGN USING VERILOG	9
Hardware Modeling with Verilog HDL – Logic System, Data Types and Operators For Modeling in Verilog HDL - Behavioral Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.		
		Total Instructional hours : 45

Course Outcomes : Students will be able to	
CO1	Analyze and design synchronous sequential digital circuits.
CO2	Analyze and design asynchronous sequential digital circuits.
CO3	Design fault diagnosis system for testing various faults.
CO4	Identify the programmable devices for system design.
CO5	Design and implement digital circuits of industry standards by using programming tools.

Reference Books

1.	Charles H. Roth Jr “Fundamentals of Logic Design”, Thomson Learning, 2004.
2.	M.D. Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 1999.
3.	M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
4.	Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
5.	Parag K.Lala, “Fault Tolerant and Fault Testable Hardware Design”, B S Publications, 2002.
6.	Parag K.Lala, “Digital system Design using PLD”, B S Publications, 2003.
7.	S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

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M.E.	M19VDT102 - CMOS DIGITAL VLSI DESIGN (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce the principle of operation of CMOS inverter.
2.	To study the concept of combinational logic circuits.
3.	To study the concept of sequential logic circuits.
4.	To introduce the architectures of VLSI system.
5.	To learn about the interconnect and clocking process.

UNIT – I	MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER	9

MOS (FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT – II	COMBINATIONAL LOGIC CIRCUITS	9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT – III	SEQUENTIAL LOGIC CIRCUITS	9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonstable Sequential Circuits.

UNIT – IV	ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES	9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT – V	INTERCONNECT AND CLOCKING STRATEGIES	9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design and Self – Timed Circuit Design.

Total Instructional hours : 45

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Course Outcomes : Students will be able to	
CO1	Outline the concept and working of CMOS inverter.
CO2	Explain the process of combinational design.
CO3	Explain the Latches and registers.
CO4	Analyze the arithmetic building blocks and memory architecture.
CO5	Outline the concept of interconnect and clocking.

Reference Books	
1.	Jan Rabaey, Anantha Chandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”, Prentice Hall of India, Second Edition, 2003.
2.	Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press, 3rd Edition, 2010.
3.	M J Smith, “Application Specific Integrated Circuits”, Addisson Wesley, 1997.
4.	N.Weste, K. Eshraghian, “Principles of CMOS VLSI Design”, Addision Wesley, Second Edition, 1993.

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M.E.	M19VDT103 - DSP INTEGRATED CIRCUITS	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To familiarize the concept of DSP and DSP algorithms.
2.	To introduction to Multirate systems and finite word length effects.
3.	To know about the basic DSP processor architectures.
4.	To study the synthesis of DSP architectures.
5.	To learn the processing elements of DSP architectures.

UNIT – I	INTRODUCTION TO DSP INTEGRATED CIRCUITS	9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT – II	DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS	9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT – III	DSP ARCHITECTURES	9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT – IV	SYNTHESIS OF DSP ARCHITECTURES	9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements – clocking of synchronous systems, Asynchronous systems – FSM.

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UNIT – V	ARITHMETIC UNIT AND PROCESSING ELEMENTS	9
Conventional number system, Redundant Number system, Residue Number System, Bit- parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor.		
		Total Instructional hours : 45

Course Outcomes : Students will be able to	
CO1	Outline the Digital Signal Processing concepts and its algorithms
CO2	Explain the concept of digital filters
CO3	Compare various DSP architectures
CO4	Analyse the DSP processor architectures and synthesis
CO5	Explain the processing elements and arithmetic unit

Reference Books	
1.	B.Venkatramani, M.Bhaskar, “Digital Signal Processors”, Tata McGraw-Hill, 2002.
2.	John J. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Pearson Education, 2002.
3.	KeshabParhi, “VLSI Digital Signal Processing Systems design & Implementation”, John Wiley & Sons, 1999.
4.	Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York, 1999.

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M.E.	M19VDT104 - CAD FOR VLSI CIRCUITS (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce the VLSI Design methodologies.
2.	To study the algorithms related to placement and partitioning.
3.	To study the various routing and floor planning algorithms.
4.	To learn the synthesis processes understand VLSI design automation tools.
5.	To study the high level synthesis.

UNIT – I	INTRODUCTION TO VLSI DESIGN FLOW	9
Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.		

UNIT – II	LAYOUT, PLACEMENT AND PARTITIONING	9
Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning.		

UNIT – III	FLOOR PLANNING AND ROUTING	9
Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.		

UNIT – IV	SIMULATION AND LOGIC SYNTHESIS	9
Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.		

UNIT – V	HIGH LEVEL SYNTHESIS	9
Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.		
Total Instructional hours : 45		

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Course Outcomes : Students will be able to	
CO1	Outline the flow of VLSI design.
CO2	Explain the algorithms related to placement and partitioning and layout rules.
CO3	Outline floor planning and routing.
CO4	Explain Simulation and Logic Synthesis.
CO5	Examine the hardware models for high level synthesis.

Reference Books	
1.	N.A. Sherwani, “Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2.	S.H. Gerez, “Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
3.	Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World Scientific, 1999.
4.	Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing, 1987.

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M.E.	M19VDT105 - ANALOG IC DESIGN	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To study MOS devices modelling and scaling effects.
2.	To familiarize the design of single stage and multistage MOS amplifier.
3.	To learn and analysis frequency responses of MOS amplifiers.
4.	To introduce the concept of current mirror.
5.	To study the OPAMP circuits.

UNIT – I	MOSFET METRICS	9

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller‟s approximation.

UNIT – II	SINGLE STAGE AND TWO STAGE AMPLIFIERS	9

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros.

UNIT – III	FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS	9

Frequency Response of Single Stage Amplifiers – Noise in Single stage Amplifiers – Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers, – Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks.

UNIT – IV	CURRENT MIRRORS AND REFERENCE CIRCUITS	9

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design.

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UNIT – V	OP AMPS	9
Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits - Low voltage OPAMP.		
		Total Instructional hours : 45

Course Outcomes : Students will be able to	
CO1	Explain the basics of MOSFET circuits.
CO2	Analyze the input and output impedances of stage amplifiers.
CO3	Examine the Stability, frequency response and Noise in MOS amplifiers.
CO4	Design the current mirror and reference circuits.
CO5	Explain the characteristics of OPAMP.

Reference Books	
1.	BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2000.
2.	Philip E.Allen, “CMOS Analog Circuit Design”, Oxford University Press, 2013.
3.	Paul R.Gray, “Analysis and Design of Analog Integrated Circuits”, Wiley Student edition, 5th edition, 2009.
4.	R.Jacob Baker, “CMOS: Circuit Design, Layout, and Simulation”, Wiley Student Edition, 2009.

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M.E.	M19VDP101 - VLSI DESIGN LABORATORY - I	T	P	TU	C
		0	4	0	2

Course Objectives	
1.	The laboratory based study for the entire program is clubbed under three categories. One is the FPGA based design methodology; the second is the simulation of analog building blocks, and analog and digital CAD design flow. Experiments pertaining to the former two topics are covered in this lab course and those pertaining to the latter will be covered in VLSI Design Lab II.
2.	FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

List of Experiments:	
Expt. No.	**Description of the Experiments**
1.	Understanding Synthesis principles. Back annotation.
2.	Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3.	FPGA real time programming and I/O interfacing.
4.	Interfacing with Memory modules in FPGA Boards.
5.	Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6.	Real time application development.
7.	Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural.

Total Instructional hours : 60

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Course Outcomes : Students will be able to	
CO1	Apply FPGA Concepts in real time applications.
CO2	Examine the input output interfacing of FPGA.
CO3	Design a FPGA based model for signal processing.
CO4	Develop a FPGA based real time model.
CO5	Outline about HDL.

List of Equipment Required

Sl. No.	Description of the Equipment	Quantity Required (Nos.)
1.	Xilinx / Equivalent EDA tool	15
2.	FPGA - Altera / Sparton boards	14
3.	Logic Analyzer	4
4.	DSO	4
5.	Interface Board - ADC	1
6.	DAC	1
7.	Motor Control	2
8.	SPICE Software	15

EXCELLENCE BEYOND EXPECTATION KIT COIMBATORE

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Semester - II

M.E.	M19VDT201 - TESTING OF VLSI CIRCUITS	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand logic fault models.
2.	To learn test generation for sequential and combinational logic circuits.
3.	To introduce testing designs.
4.	To learn testing algorithms.
5.	To study about the fault diagnosis.

UNIT – I	TESTING AND FAULT MODELLING	9
Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.		

UNIT – II	TEST GENERATION 9	9
Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.		

UNIT – III	DESIGN FOR TESTABILITY	9
Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.		

UNIT – IV	SELF – TEST AND TEST ALGORITHMS	9
Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.		

UNIT – V	FAULTDIAGNOSIS	9
Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.		
		Total Instructional hours : 45

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Course Outcomes : Students will be able to	
CO1	Outline the testing and fault modelling.
CO2	Explain the test generation for combinational and sequential circuits.
CO3	Analyse the various testing designs.
CO4	Make use of the testing algorithm.
CO5	Explain fault diagnosis.

Reference Books	
1.	A.L.Crouch, “Design Test for Digital ICs and Embedded Core Systems”, Prentice Hall International, 2002.
2.	M. Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
3.	M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed - Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4.	P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

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M.E.	M19VDT202 - VLSI SIGNAL PROCESSING (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To learn typical DSP algorithms.
2.	To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
3.	To introduce efficient design of DSP architectures suitable for VLSI.
4.	To study about numerical strength reduction.

UNIT – I	PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS	9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT – II	ALGORITHMIC STRENGTH REDUCTION TECHNIQUE	9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT – III	ALGORITHIMIC STRENGTH REDUCTION - II	9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT – IV	BIT - LEVEL ARITHMETIC ARCHITECTURES	9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry - ripple and carry - save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner"s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

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UNIT – V	NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING	9
Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.		
Total Instructional hours : 45		

Course Outcomes : Students will be able to	
CO1	Outline the pipelining and parallel processing of DSP filters.
CO2	Explain the first level strength reduction techniques.
CO3	Explain the first level strength reduction techniques.
CO4	Analyze the various bit level arithmetic architectures.
CO5	Explain the numerical strength reduction and pipelining process of filters.

Reference Books	
1.	Keshab K. Parhi, “VLSI Digital Signal Processing Systems, Design and implementation”, Wiley, Interscience, 2007.
2.	U. Meyer – Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004.

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M.E.	M19VDT203 - LOW POWER VLSI DESIGN	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To identify sources of power in an IC.
2.	To identify the power reduction techniques based on technology independent and technology dependent.
3.	To study the low power CMOS circuits.
4.	To learn suitable techniques for power estimation.
5.	To design circuits with low power dissipation.

UNIT – I	POWER DISSIPATION IN CMOS	9

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques for Leakage Power Reduction - Basic principle of low power design.

UNIT – II	POWER OPTIMIZATION	9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures- BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison.

UNIT – III	DESIGN OF LOW POWER CMOS CIRCUITS	9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT – IV	POWER ESTIMATION	9

Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

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UNIT – V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	9
Synthesis for low power – Behavioral level transform – software design for low power.		
		Total Instructional hours : 45

Course Outcomes : Students will be able to	
CO1	Explain the basics and advanced techniques in low power design.
CO2	Explain the concept of power optimization.
CO3	Model the low power circuits.
CO4	Analyse the power estimation techniques.
CO5	Design the software models for low power.

Reference Books	
1.	Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
2.	A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer, 1995.
3.	DimitriosSoudris, C.Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
4.	Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
5.	James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc., 2001.
6.	J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
7.	Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
8.	Kiat-send Yeo, Kaushik Roy, “Low-Voltage, Low-power VLSI Subsystem”, Tata McGraw-Hill, 2009.

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M.E.	M19VDP201 - VLSI DESIGN LABORATORY - II	T	P	TU	C
		0	4	0	2

Course Objectives	
1.	The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use of this design flow in some for or the other. Proficiency and familiarity with the various stages of a typical „state of this design flow is a prerequisite for any student who wishes to be a part of either the industry or their search in VLSI over one full semester exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of simulation, and power and clock routing modules. ASIC RTL realization of an available open source MCU.

List of Experiments:	
Expt. No.	**Description of the Experiments**
1.	To synthesize and understand the Boolean optimization in synthesis.
2.	Static timing analyses procedures and constraints.
3.	Critical path considerations.
4.	Scan chain insertion, Floor planning, Routing and Placement procedures.
5.	Power planning, Layout generation, LVS, back annotation and Total power estimate.
6.	Analog circuit simulation.
7.	Simulation of logic gates, Current mirrors, Current sources and Differential amplifier in Spice.
8.	Layout generations, LVS and Back annotation
	Total Instructional hours : 60

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Course Outcomes : Students will be able to	
CO1	Apply Boolean optimization concept.
CO2	Analyze the timing constraints and procedures.
CO3	Examine various floor planning, routing and placement procedures.
CO4	Test the analog circuits.
CO5	Explain about layout generations.

List of Equipment Required		
Sl. No.	**Description of the Equipment**	**Quantity Required (Nos.)**
1.	CADENCE / TANNER / Mentor Graphics / Synopses / SPICE Software	15

EXCELLENCE BEYOND EXPECTATION KIT COIMBATORE

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M.E.	M19CEP201 - ARTICLE WRITING AND SEMINAR	T	P	TU	C
		0	2	0	1

Course Objectives	
In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps :	
1.	Selecting a subject, narrowing the subject into a topic.
2.	Stating an objective.
3.	Collecting the relevant bibliography (at least 15 journal papers).
4.	Preparing a working outline.
5.	Studying the papers and understanding the author's contributions and critically analysing each paper.
6.	Preparing a working outline.
7.	Linking the papers and preparing a draft of the paper.
8.	Preparing conclusions based on the reading of all the papers.
9.	Writing the Final Paper and giving final Presentation.

Please keep a file where the work carried out by you is maintained. Activities to be carried out

Activity	Instructions	Submission Week	Evaluation Week
Selection of area of interest and Topic (Stating an Objective)	You are requested to select an area of interest, topic and state an objective	2nd week	3 % Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals	3rd week	3% (the selected information must be area specific and of international and national standard)

BoS Chairman

	3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.		
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar When picking papers to read - try to: Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, Favour papers from well-known journals and conferences, Favour "first" or "foundational" papers in the field	4th week	6% (the list of standard papers and reason for selection)

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	(as indicated in other people‟s survey paper), Favour more recent papers, Pick a recent survey of the field so you can quickly gain an overview, Find relationships with respect to each other and to your topic area (classification scheme/categorization) Mark in the hard copy of papers whether complete work or section/sections of the paperare being considered		
Reading and notes for first 5 papers	Reading Paper Process For each paper form a Table answering the following questions: What is the main topic of the article? What was/were the main issue(s) the author said they want to discuss? Why did the author claim it was important? How does the work build on other‟s work, in the author‟s opinion? What simplifying assumptions does the author claim to be making?	5th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

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	What did the author do? How did the author claim they were going to evaluate their work and compare it to others? What did the author say were the limitations of their research? What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next 5 papers	Repeat Reading Paper Process	6th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

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Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	8% (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	6% (Clarity, purpose and conclusion) 6% Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	5% (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11th week	10% (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	5% (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	10% (based on presentation and Viva-voce)

Course Outcomes : Students will be able to	
CO1	Survey the relevant information.
CO2	Outline the importance's.
CO3	Formulate the concept.
CO4	Compare the data's with existing.
CO5	Outline about concluding remarks.

BoS Chairman

Professional Elective - I

M.E.	M19VDE201 - DEVICE MODELLING (Common to VLSI & AE)	T	P	TU	C
		0	2	0	1

Course Objectives	
1.	To study the MOS capacitors and to model MOS Transistors.
2.	To learn about the MOSFET characteristics.
3.	To understand the various CMOS design parameters and their impact on performance of the device.
4.	To study the device level characteristics of BJT transistors.

UNIT – I	MOS CAPACITORS	9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non-equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT – II	MOSFET DEVICES	9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I-V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short - Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source – Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields.

UNIT – III	CMOS DEVICE DESIGN	9

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Non- scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non-uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

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UNIT – IV	CMOS PERFORMANCE FACTORS	9
Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS.		

UNIT – V	BIPOLAR DEVICES	9
N–P–N Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base– Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non- ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BVCEO and BVCBO.		
Total Instructional hours: 45		

Course Outcomes : Students will be able to	
CO1	Outline the concept of MOS capacitors.
CO2	Explain the operation of MOSFET with its characteristics.
CO3	Design and model MOSFET device to desired specifications.
CO4	Analyze the performance metrics of CMOS.
CO5	Design and model BJT device to desired specifications.

Reference Books	
1.	Behzad Razavi, “Fundamentals of Microelectronics”, Wiley Student Edition, 2nd Edition.
2.	J P Collinge, C. A. Collinge, “Physics of Semiconductor devices”, Springer, 2002.
3.	Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition.

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M.E.	M19AEE101 - COMPUTER ARCHITECTURE AND PARALLEL PROCESSING (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To study various types of processor architectures and the importance of scalable architectures.
2.	To introduce parallel processing and pipelining.
3.	To learn about the memory hierarchy.
4.	To study the multiprocessor architecture.
5.	To study the multicore architecture.

UNIT – I	COMPUTER DESIGN AND PERFORMANCE MEASURES	9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures.

UNIT – II	PARALLEL PROCESSING, PIPELINING AND ILP	9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors -Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.

UNIT – III	MEMORY HIERARCHY DESIGN	9

Memory Hierarchy - Meemory Technology and Optimizations – Cache memory – Optimizations of Cach Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT – IV	MULTIPROCESSORS	9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

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UNIT – V	MULTI-CORE ARCHITECTURES	9
Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture- hp architecture.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Explain the multiprocessors and its performance measure.
CO2	Explain the concept of parallel processing and pipelining.
CO3	Analyze about the memory hierarchy design.
CO4	Outline the issues related to multiprocessors.
CO5	Compare multicore architectures.

Reference Books	
1.	David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware / software approach”, Morgan Kaufmann / Elsevier, 1997
2.	Dimitrios Soudris, Axel Jantsch,“Scalable Multi-core Architectures : Design Methodologies and Tools”, Springer, 2012.
3.	Hwang Briggs, “Computer Architecture and parallel processing”, McGraw Hill, 1984.
4.	John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”, Morgan Kaufmann / Elsevier, 4th Edition, 2007.
5.	John P. Hayes, “Computer Architecture and Organization”, McGraw Hill, 3rd Edition, 1998.
6.	John P. Shen, “Modern processor design : Fundamentals of super scalar processors”, Tata McGraw Hill, 2003.
7.	Kai Hwang, “Advanced Computer Architecture”, McGraw Hill International, 2001.
8.	William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Seventh Edition, 2006.

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M.E.	M19AET301 - ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURE (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To study 80486 and Pentium processor.
2.	To understand CISC and RISC Architectures.
3.	To learn ARM processor.
4.	To learn ARM instruction set.
5.	To study about microcontroller.

UNIT – I	80486 AND PENTIUM PROCESSOR	9

80486 PROCESSOR: Basic programming model – Memory organization – Data types – Instruction set - Addressing mode – Address translation – Interrupts –PENTIUM PROCESSOR Introduction to Pentium processor architecture – Special Pentium Registers-Pentium Memory Management – Introduction to Pentium pro processor – Pentium Pro Special Features.

UNIT – II	CISC AND RISC ARCHITECTURE	9

Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000–SPARC – Intel i860 - IBM RS/6000.

UNIT – III	ARM PROCESSOR	9

ARM Programmer's Model – Registers – Processor Modes – State of the processor – Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Typical 3 stage pipelined ARM organization–Introduction to ARM Memory Management Unit, Case Study.

UNIT – IV	ARM ADDRESSING MODES AND INSTRUCTION SET	9

ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set Overview – LPC210X ARM Processor Features, Case Study.

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UNIT – V	PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER	9
Instruction set, addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART. **MOTOROLA :** CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter – PWM, Case Study.		
Total Instructional hours: 45		

Course Outcomes : Students will be able to	
CO1	Outline the basics of 80486 processor.
CO2	Explain the functionalities of CISC and RISC architecture.
CO3	Analyze the functionalities of ARM processor.
CO4	Outline ARM instruction set.
CO5	Explain PIC microcontroller and Motorola 68HC11 microcontroller.

Reference Books

1.	Andrew Sloss, “ARM System Developers Guide”, Morgan Kaufmann Publishers, 2005 approach, Morgan Kaufmann / Elsevier, 1997.
2.	Barry B Brey, “The Intel Microprocessor, Pentium and Pentium Pro Processor, Architecture Programming and Interfacing”, Prentice Hall of India, 2002.
3.	Daniel Tabak, “Advanced Microprocessors”, McGraw Hill Inc., 1995.
4.	David E Simon “An Embedded Software Primer”, Pearson Education, 2007.
5.	Gene .H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.
6.	Intel, “Microprocessors”, Vol-I & Vol-II, Intel Corporation, USA, 1992.
7.	John .B.Peatman , “Design with PIC Microcontroller” , Prentice hall, 1997.
8.	Mohammed Rafiquzzaman, “Microprocessors and Microcomputer Based System Design”, Universal Book Stall, New Delhi, 1990.
9.	Steve Furber, “ARM System-on-Chip Architecture”, Pearson Education, 2005.
10.	“ARM7 TDMI Technical Reference Manual”, ARM Ltd., UK, 2004.

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M.E.	M19AEE103 - NEURAL NETWORKS AND APPLICATIONS (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce the artificial neural network concepts.
2.	To study various types of artificial neural network architectures.
3.	To study advanced artificial neural network concepts.

UNIT – I	INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS	9
Neuro-physiology - General Processing Element - ADALINE - LMS learning rule - MADALINE – MR2 training algorithm.		

UNIT – II	BPN AND BAM	9
Back Propagation Network - updating of output and hidden layer weights -application of BPN – associative memory - Bi-directional Associative Memory - Hopfield memory - traveling sales man problem.		

UNIT – III	SIMULATED ANNEALING AND CPN	9
Annealing, Boltzmann machine - learning - application - Counter Propagation network - architecture -training - Applications.		

UNIT – IV	SOM AND ART	9
Self organizing map - learning algorithm - feature map classifier - applications - architecture of Adaptive Resonance Theory - pattern matching in ART network.		

UNIT – V	NEOCOGNITRON	9
Architecture of Neocognitron - Data processing and performance of architecture of spacio – temporal networks for speech recognition.		
		Total Instructional hours: 45

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Course Outcomes : Students will be able to	
CO1	Explain the concepts of neural networks and different training / learning algorithms.
CO2	Design BPNN to solve real time problems.
CO3	Apply the concept of counter propagation network for various applications.
CO4	Illustrate problem-solving based on pattern matching with specified Self Organizing Map algorithm.
CO5	Apply spatial - temporal networks for speech recognition.

Reference Books	
1.	J.A. Freeman and B.M. Skapura, “Neural Networks, Algorithms Applications and Programming Techniques”, Addison-Wesely, 2003.
2.	Laurene Fausett, “Fundamentals of Neural Networks: Architecture, Algorithms and Applications”, Prentice Hall, 2004.
3.	Simon Haykin, “Neural Networks & Learning Machines”, Pearson Education, 3rd Edition, 2011.
4.	Martin T. Hagan, Howard B. Demuth, Mark Beale, “Neural Network Design”, Thomson and Learning, Third Reprint, 2008.

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Professional Elective - II

M.E.	M19VDE202- ASIC AND FPGA DESIGN (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To study the different types of ASIC and PLD.
2.	To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC.
3.	To familiarize the different types of programming technologies and testing.
4.	To learn the architecture of different types of FPGA.
5.	To gain knowledge about SoC.

UNIT – I	OVERVIEW OF ASIC AND PLD	9
Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs.		

UNIT – II	ASIC PHYSICAL DESIGN	9
System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC.		

UNIT – III	LOGIC SYNTHESIS, SIMULATION AND TESTING	9
Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.		

UNIT – IV	FIELD PROGRAMMABLE GATE ARRAYS	9
FPGA Design: FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.		

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UNIT – V	SOC-DESIGN	9
System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	:Outline about various types of ASICs and PLDs.
CO2	Analyze the physical design steps of ASIC.
CO3	Explain the logic synthesis, simulation and testing.
CO4	Analyze the FPGA.
CO5	Explain the design issues of SOC.

Reference Books	
1.	David A. Hodges, “Analysis and Design of Digital Integrated Circuits (3/e)”, MGH, 2004.
2.	H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.
3.	Jan. M. Rabaey et al, “Digital Integrated Circuit Design Perspective (2/e)”, PHI, 2003.
4.	M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson, 2003.
5.	J. Old Field, R.Dorf, “Field Programmable Gate Arrays”, John Wiley & Sons, Newyork.
6.	P.K.Chan & S. Mourad, “Digital Design using Field Programmable Gate Array”, Prentice Hall.
7.	Sudeep Pasricha and Nikil Dutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsevier, 2008.
8.	S.Trimberger, Edr, “Field Programmable Gate Array Technology”, Kluwer Academic Pub.
9.	S.Brown,R.Francis, J.Rose, Z.Vransic, “Field Programmable Gate Array”, Kluwer Pub.
10.	Richard F. Jinder , “Engineering Digital Design”, Academic press.

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M.E.	M19VDE203 - NANO ELECTRONICS (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand the semiconductor nano devices.
2.	To study the materials involved in nano devices.
3.	To learn the operation of nano thermal sensors.
4.	To understand various materials used in gas sensors.
5.	To study the operation of bio sensor.

UNIT – I	SEMICONDUCTOR NANO DEVICE S	9

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single - Electron Transistors; Nanorobotics and Nano manipulation; Mechanical Molecular Nano devices; Nano computers: Optical Fibers for Nano devices; Photochemical Molecular Devices; DNA - Based Nano devices; Gas - Based Nano devices.

UNIT – II	ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS	9

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs - High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT – III	THERMAL SENSORS	9

Thermal energy sensors - temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT – IV	GAS SENSOR MATERIALS	9

Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity, Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

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UNIT – V	BIOSENSORS	9
Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Classify the types of Nano devices.
CO2	Analyze the materials used in Nano device.
CO3	Explain the operation of thermal sensor.
CO4	Examine the operation of gas sensor.
CO5	Outline the operation of bio sensor.

Reference Books	
1.	K.E. Drexler, “Nano systems”, Wiley, 1992.
2.	M.C. Petty, “Introduction to Molecular Electronics”, 1995.
3.	W. Ranier, “Nano Electronics and Information Technology”, Wiley, 2003.

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M.E.	M19AEE201- HIGH PERFORMANCE NETWORKS (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce various systems related to networks.
2.	To study the applications of multimedia networks.
3.	To learn the concept of advanced networks.
4.	To study the various traffic modeling.
5.	To learn about network security in many layers and network management.

UNIT – I	INTRODUCTION	9
Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.		

UNIT – II	MULTIMEDIA NETWORKING APPLICATIONS	9
Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.		

UNIT – III	ADVANCED NETWORKS CONCEPTS	9
VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks- P2P connections.		

UNIT – IV	TRAFFIC MODELLING	9
Little"s theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.		

UNIT – V	NETWORK SECURITY AND MANAGEMENT	9
Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1.		
Total Instructional hours: 45		

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Course Outcomes : Students will be able to	
CO1	Outline the basic high performance network systems.
CO2	Explain the applications of multimedia networks.
CO3	Analyse the concepts of advanced networks.
CO4	Outline the traffic modelling.
CO5	Analyse the network security methods.

Reference Books	
1.	Aunurag Kumar, D. M Anjunath, Joy Kuri, “Communication Networking”, Morgan Kaufmann Publishers, 1st Edition, 2004.
2.	Fred Halsall and Lingana Gouda Kulkarni, “Computer Networking and the Internet”, Pearson Education, 5th Edition, 2006.
3.	Hersent Gurle & Petit, “IP Telephony, packet Pored Multimedia communication Systems”, Pearson Education, 2003.
4.	J.F. Kurose & K.W. Ross, “Computer Networking- A top down approach featuring the internet”, Pearson, 2nd Edition, 2003.
5.	Larry l.Peterson & Bruce S.David, “Computer Networks: A System Approach”, 1996.
6.	LEOM-GarCIA, WIDJAJA, “Communication networks”, TMH seventh, Reprint, 2002.
7.	Nader F. Mir, “Computer and Communication Networks”, First edition, 2010.
8.	Walrand J. Varatya, “High performance communication network”, Morgan Kauffman – Harcourt Asia Pvt. Ltd., 2nd Edition, 2000.

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M.E.	M19AEE202 - WIRELESS ADHOC AND SENSOR NETWORKS (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand the basics of Ad-hoc, Sensor Networks and various fundamental and emerging protocols of all layers.
2.	To study about the routing architecture of sensor networks.
3.	To understand the nature and applications of Ad-hoc and sensor networks.
4.	To understand various security practices and protocols of Ad-hoc and Sensor networks.

UNIT – I	MAC & TCP IN AD HOC NETWORKS	9

Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.

UNIT – II	ROUTING IN AD HOC NETWORKS	9

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT – III	MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS	9

Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support.

UNIT – IV	SENSOR MANAGEMENT	9

Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.

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UNIT – V	SECURITY IN AD HOC AND SENSOR NETWORKS	9
Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defense against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Explain the protocols developed for ad hoc and sensor networks.
CO2	Analyse different routing approaches.
CO3	Outline different architecture in ad hoc and sensor networks.
CO4	Build a Sensor network environment for different type of applications.
CO5	Analyse about the security in sensor networks.

Reference Books	
1.	Adrian Perrig, J. D. Tygar, “Secure Broadcast Communication: In Wired and Wireless Networks”, Springer, 2006.
2.	Carlos De Morais Cordeiro, Dharma Prakash Agrawal “Ad Hoc and Sensor Networks: Theory and Applications”, World Scientific Publishing, 2nd Edition, 2011.
3.	C.Siva Ram Murthy and B.S.Manoj, “Ad Hoc Wireless Networks – Architectures and Protocols”, Pearson Education, 2004.
4.	C.K.Toh, “Ad Hoc Mobile Wireless Networks”, Pearson Education, 2002.
5.	Erdal Çayırcı, Chunming Rong, “Security in Wireless Ad Hoc and Sensor Networks”, John Wiley and Sons, 2009.
6.	Holger Karl, Andreas willig, “Protocols and Architectures for Wireless Sensor Networks”, John Wiley & Sons, Inc., 2005.
7.	Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, “Ad Hoc Mobile Wireless Networks”, Auerbach Publications, 2008.
8.	Waltenegus Dargie, Christian Poellabauer, “Fundamentals of Wireless Sensor Networks Theory and Practice”, John Wiley and Sons, 2010.

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Professional Elective - III

M.E.	M19VDE204 - SYSTEM ON CHIP DESIGN (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce SoC concepts.
2.	To study the system level modelling.
3.	To learn the hardware/software co-design principles.
4.	To familiar with system synthesis.
5.	To learn the hardware/software co-verification principles.

UNIT – I	INTRODUCTION	9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design.

UNIT – II	SYSTEM LEVEL MODELLING	9

System C : overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples.

UNIT – III	HARDWARE SOFTWARE CO-DESIGN	9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT – IV	SYNTHESIS	9

System synthesis: Transaction Level Modelling (TLM) based design, automaticTLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling.

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UNIT – V	SOC VERIFICATION AND TESTING	9
SoC and IP integration, Verification: Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modelling, test power dissipation, test access mechanism, Case Study.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Outline the basics of SoC design.
CO2	Explain the modelling process.
CO3	Analyse and design the software hardware models.
CO4	Explain the synthesis process.
CO5	Design the test mechanism for SoC test and verification.

Reference Books	
1.	D. Black, J. Donovan, “System C : From the Ground Up”, Springer, 2004.
2.	D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, “Embedded System Design : Modeling, Synthesis,Verification”, Springer, 2009.
3.	C.Siva Ram Murthy and B.S.Manoj, “Ad Hoc Wireless Networks – Architectures and Protocols”, Pearson Education, 2004.
4.	Erik Larson, “Introduction to advanced system-on-chip test design and optimization”, Springer, 2005.
5.	Grotker, T., Liao, S., Martin, G. & Swan, S., “System design with System C”, Springer, 2002.
6.	Holger Karl, Andreaswillig, “Protocols and Architectures for Wireless Sensor Networks”, John Wiley & Sons, Inc., 2005.
7.	Ghenassia, F., “Transaction-level modeling with System C: TLM concepts and applications for embedded systems”, Springer, 2010.
8.	Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, “Low power NoC for high performance SoC design”, CRC press, 2008.

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9.	M. L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits”, Springer, 2005.
10.	M. Abramovici, M. Breuer, and A. Friedman, “Digital System Testing and Testable Design”, IEEE Press, 1994.
11.	P. Marwedel, “Embedded System Design”, Springer, 2003.
12.	Prakash Rashinkar, Peter Paterson and Leena Singh, “System-on-a chip verification: Methodology and techniques”, kluwer Academic Publishers, 2002.
13.	T. Noergaard, “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”, Newness.
14.	Vijay K. Madisetti Chonlameth Arpikanondt, “A Platform-Centric Approach to System- on-Chip (SOC) Design”, Springer, 2005.
15.	Youn-Long Steve Lin, “Essential Issues in SOC Design Designing Complex Systems- on-Chip”, Springer, 2006.

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M.E.	M19AET201- SOFT COMPUTING AND OPTIMIZATION TECHNIQUES (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand various neural networks and learning methods.
2.	To overview of Fuzzy logic.
3.	To study the concept of Neuro – Fuzzy modeling.
4.	To introduce the optimization techniques.

UNIT – I	NEURAL NETWORKS	9
Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network.		

UNIT – II	FUZZY LOGIC	9
Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making.		

UNIT – III	NEURO-FUZZY MODELING	9
Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – Case Studies.		

UNIT – IV	CONVENTIONAL OPTIMIZATION TECHNIQUES	9
Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton‟s Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.		

UNIT – V	EVOLUTIONARY OPTIMIZATION TECHNIQUES	9
Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.		
		Total Instructional hours: 45

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Course Outcomes : Students will be able to	
CO1	Outline the basics of neural network and learning methods.
CO2	Outline the basics of fuzzy logic.
CO3	Examine machine learning through Neural Fuzzy concept.
CO4	Explain the conventional optimization techniques.
CO5	Explain the evolutionary optimization techniques.

Reference Books	
1.	David E. Goldberg, “Genetic Algorithms in Search, Optimization and Machine learning”, Addison wesley, 2009.
2.	George J. Klir and Bo Yuan, “Fuzzy Sets and Fuzzy Logic-Theory and Applications”, Prentice Hall, 1995.
3.	James A. Freeman and David M. Skapura, “Neural Networks Algorithms, Applications, and Programming Techniques”, Pearson Edn., 2003.
4.	Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, “Neuro-Fuzzy and Soft Computing”, Prentice-Hall of India, 2003.
5.	Mitchell Melanie, “An Introduction to Genetic Algorithm”, Prentice Hall, 1998.
6.	Simon Haykins, “Neural Networks: A Comprehensive Foundation”, Prentice Hall International Inc, 1999.
7.	Singiresu S. Rao, “Engineering optimization Theory and practice”, John Wiley & sons, inc, Fourth Edition, 2009.
8.	Timothy J.Ross, “Fuzzy Logic with Engineering Applications”, McGraw-Hill, 1997.
9.	Venkata Rao, Vimal J. Savsani, “Mechanical Design Optimization Using Advanced Optimization Techniques”, Springer, 2012.

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M.E.	M19VDE205 - RECONFIGURABLE ARCHITECTURES	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce processors and architectures.
2.	To learn about programmed FPGAs.
3.	To study various routing in FPGAs.
4.	To introduce design styles for FPGA.
5.	To familiar with SoPC designs.

UNIT – I	INTRODUCTION	9

Domain-specific processors, Application specific processors, Reconfigurable Computing Systems – Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture- fine, coarse grain & hybrid architectures – Examples.

UNIT – II	FPGA TECHNOLOGIES & ARCHITECTURE	9

Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.

UNIT – III	ROUTING FOR FPGAS	9

General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability- Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks.

UNIT – IV	HIGH LEVEL DESIGN	9

FPGA Design style: Technology independent optimization- technology mapping- Placement. High-level synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.

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UNIT – V	APPLICATION DEVELOPMENT WITH FPGAS	9
Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Illustrate the concepts of reconfigurable architectures.
CO2	Explain the FPGA technologies.
CO3	Analyze the various routing technologies.
CO4	Explain the design styles of FPGA.
CO5	Apply the FPGA techniques in solving the real world problems.

Reference Books	
1.	Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010.
2.	Clive Maxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools and Flows”, Newnes, Elsevier, 2006.
3.	Jorgen Staunstrup, Wayne Wlf, “Hardware/Software Co- Design: Principles and practice”, Kluwer Academic Pub, 1997.
4.	Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
5.	Russell tessier and Wayne Burleson, “Reconfigurable Computing for Digital Signal Processing: A Survey”, Journal of VLSI Signal processing, 28, p7-27, 2001.
6.	Stephen M. Trimberger, “Field – programmable Gate Array Technology”, Springer, 2007.
7.	Stephen D. broen, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, “Field programmable Gate Arrays”, Kluwer Academic Publishers, 1992.
8.	Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing –The Theory and Practice of FPGA - Based Computation”, Elsevier / Morgan Kaufmann, 2008.

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M.E.	M19VDE206 - SIGNAL INTEGRITY FOR HIGH SPEED NETWORKS	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To study the various propagation requirements of transmission lines.
2.	To learn about the multi conductor transmission lines.
3.	To identify the non ideal effects of transmission lines.
4.	To familiar about the design of transmission line system.
5.	To study the effect of oscillators in transmission lines.

UNIT – I	SIGNAL PROPAGATION ON TRANSMISSION LINES	9

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT – II	MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS TALK	9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT – III	NON-IDEAL EFFECTS	9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors

UNIT – IV	POWER CONSIDERATIONS AND SYSTEM DESIGN	9

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate ,Timing analysis.

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UNIT – V	CLOCK DISTRIBUTION AND CLOCK OSCILLATORS	9
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Make use of the wave propagation concepts.
CO2	Explain about various parameters involved in wave propagation.
CO3	Identify the various effects in wave propagation.
CO4	Analyse the power issues, jitter and filtering in wave propagation.
CO5	Analyse the clocking system for signal transmission.

Reference Books	
1.	Douglas Brooks, “Signal Integrity Issues and Printed Circuit Board Design”, Prentice Hall PTR, 2003.
2.	Eric Bogatin, “Signal Integrity – Simplified”, Prentice Hall PTR, 2003.
3.	H. W. Johnson and M. Graham, “High-Speed Digital Design: A Handbook of Black Magic”, Prentice Hall, 1993.
4.	S. Hall, G. Hall, and J. McCall, “High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices”, Wiley-Interscience, 2000.

TOOLS REQUIRED	
1.	SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2.	HSPICE from synopsis, www.synopsys.com/products/mixedsignal/hspice/hspice.html
3.	SPECCTRAQUEST from Cadence, http://www.specctraquest.com

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Semester - III

M.E.	M19VDT301 - ANALOG TO DIGITAL INTERFACES	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand the importance of sampling the input analog signal for digitization and enabling circuit architectures.
2.	To learn the switched capacitor circuits and comparators.
3.	To study the principles of Analog to Digital conversion of signals.
4.	To understand the principles of Digital to Analog conversion of signals.
5.	To study the importance of calibration techniques for achieving precision during data conversion.

UNIT – I	SAMPLE AND HOLD CIRCUITS	9
Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.		

UNIT – II	SWITCHED CAPACITOR CIRCUITS AND COMPARATORS	9
Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.		

UNIT – III	DIGITAL TO ANALOG CONVERSION	9
Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture, Case Study.		

UNIT – IV	ANALOG TO DIGITAL CONVERSION	9
Performance metric, flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture, Case Study.		

UNIT – V	PRECISION TECHNIQUES	9
Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.		
		Total Instructional hours: 45

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Course Outcomes : Students will be able to	
CO1	Outline the sampling of analog signal for digitization and enabling circuit architectures.
CO2	Explain switched capacitor circuits and comparators.
CO3	Design Digital to Analog data converters based on data precision requirements.
CO4	Design Analog to Digital data converters based on data precision requirements.
CO5	Explain the offset cancellation techniques.

Reference Books	
1.	Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

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Professional Elective - IV

M.E.	M19VDE301 - PRINCIPLES OF REMOTE SENSING	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To learn physics of remote sensing.
2.	To learn data acquisition.
3.	To study about microwave remote sensing.
4.	To study the principles of thermal sensing.
5.	To learn different technique in data analysis.

UNIT – I	PHYSICS OF REMOTE SENSING	9

Introduction of Remote Sensing - Electro Magnetic Spectrum, Physics of Remote Sensing - Effects of Atmosphere - Scattering – Different types – Absorption-Atmospheric window - Energy interaction with surface features – Spectral reflectance of vegetation, soil ,and water – atmospheric influence on spectral response patterns - multi concept in Remote sensing.

UNIT – II	DATA ACQUISITION	9

Types of Platforms – different types of aircrafts-Manned and Unmanned spacecrafts – sun synchronous and geo synchronous satellites – Types and characteristics of different platforms – LANDSAT, SPOT, IRS, INSAT, IKONOS, QUICKBIRD etc - Photographic products, B/W, colour, colour IR film and their characteristics – resolving power of lens and film - Opto mechanical electro optical sensors – across track and along track scanners – multi spectral scanners and thermal scanners – geometric characteristics of scanner imagery - calibration of thermal scanners.

UNIT – III	SCATTERING SYSTEM	9

Microwave scatterometry – types of RADAR – SLAR – resolution - range and azimuth – real aperture and synthetic aperture RADAR. Characteristics of Microwave imagestopographic effect - different types of Remote Sensing platforms – airborne and space borne sensors – ERS, JERS, RADARSAT, RISAT - Scatterometer, Altimeter- LiDAR remote sensing, principles, applications.

UNIT – IV	THERMAL SENSING	9

Sensors characteristics - principle of spectroscopy - imaging spectroscopy - field conditions, compound spectral curve, Spectral library, radiative models, processing procedures, derivative spectrometry, thermal remote sensing – thermal sensors, principles, thermal data processing, applications.

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UNIT – V	DATA ANALYSIS	9
Resolution – Spatial, Spectral, Radiometric and temporal resolution- signal to noise ratio- data products and their characteristics - visual and digital interpretation –Basic principles of data processing – Radiometric correction – Image enhancement – Image classification – Principles of LiDAR, Aerial Laser Terrain Mapping.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Explain the physics behind remote sensing and understand the different remote sensing platforms used.
CO2	Examine the data acquisition process.
CO3	Explain the concepts of microwave remote sensing.
CO4	Analyse the sensors used in thermal sensing and its principle.
CO5	Outline remote sensing data analysis methods.

Reference Books	
1.	Lillesand T.M, and Kiefer,R.W, “Remote Sensing and Image interpretation”, VI Edition of John Wiley & Sons, 2000.
2.	John R. Jensen, “Introductory Digital Image Processing: A Remote Sensing Perspective”, 2nd Edition, 1995.
3.	John A.Richards, “Remate Sensing Digital Image Analysis”, Springer –Verlag,1999
4.	Paul Curran P.J, “Principles of Remote Sensing”, ELBS, 1995.
5.	Charles Elachi and Jakob J. van Zyl, “Introduction To The Physics and Techniques of Remote Sensing”, Wiley Series in Remote Sensing and Image Processing, 2006.
6.	Sabins, F.F.Jr, “Remote Sensing Principles and Image interpretation”, W.H.Freeman & Co, 1978.

BoS Chairman

M.E.	M19AEE303 - ADVANCED DIGITAL IMAGE PROCESSING (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand the fundamentals of digital image processing.
2.	To learn concept of color image processing technique.
3.	To learn morphological image processing algorithms.
4.	To learn segmentation algorithms and descriptors for image processing.
5.	To study object recognition and image processing applications.

UNIT – I	FUNDAMENTALS OF DIGITAL IMAGE PROCESSING	9

Elements of Visual Perception- Image acquisition, digitization - Histogram - Image enhancement – Spatial filters for smoothing and sharpening – Discrete 2D transforms - DFT, DCT, Walsh - Hadamard, Slant, KL, Wavelet Transform – Haar wavelet.

UNIT – II	COLOR IMAGE PROCESSSING	9

Color Image Fundamentals - Color Models - RGB, CMY, CMYK and HSI Color Models - Pseudocolor Image Processing - Intensity Slicing- Intensity to Color transformations -Basics of Color Image Processing - Color Transformation - Color Image Smoothing and Sharpening- Color Segmentation - Noise in Color Images.

UNIT – III	MORPHOLOGICAL IMAGE PROCESSING	9

Preliminaries - Basic Concepts from Set Theory - Logic Operations Involving Binary Images - Dilation and Erosion – Opening and Closing - Hit-or-Miss Transformation - Basic Morphological Algorithms - Boundary Extraction - Region Filling - Extraction of Connected Components - Convex Hull - Thinning - Thickening - Skeletons - Pruning- - Gray-Scale Morphology, Case Study.

UNIT – IV	SEGMENTATION, REPRESENTATION AND DESCRIPTION	9

Edge Detection - Edge Linking and Boundary Detection -Thresholding - Segmentation by Morphological Watershed Segmentation Algorithm - Use of Markers- Representation and Boundary Descriptors, Case Study.

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UNIT – V	OBJECT RECOGNITION AND IMAGE PROCESSING APPLICATIONS	9
Patterns and Pattern Classes - Recognition Based on Decision - Theoretic Methods – Matching Optimum Statistical Classifiers - Neural Networks, Fuzzy Systems - GA. Image compression - JPEG, JPEG 2000 JBIG standards - Watermarking – Steganography.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Explain about image acquisition, digitization and spatial filters for enhancement.
CO2	Outline color image processing techniques.
CO3	Apply morphological image processing algorithms.
CO4	Apply segmentation algorithms and descriptors for image processing.
CO5	Examine neural networks, fuzzy logic, genetic algorithms in object recognition, compression, watermarking and steganography algorithms to images.

Reference Books	
1.	Rafael C. Gonzalez, “Digital Image Processing”, Pearson Education, Inc., 3rd Edition, 2008.
2.	Milman Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing, Analysis and Machine Vision”, Brooks/Cloe, Vikas Publishing House, 2nd Edition, 1999.
3.	Khalid Sayood, “Data Compression”, Morgan Kaufmann Publishers (Elsevier)., 3rd Edition, 2006.
4.	Rafael C. Gonzalez, Richards E.Woods, Steven Eddins, “Digital Image Processing using MATLAB”, Pearson Education Inc., 2004.
5.	Willam K.Pratt, “Digital Image Processing”, John Wiley, New York, 2002.

BoS Chairman

M.E.	M19AEE304 - PATTERN RECOGNITION (Common to AE & VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To learn about supervised pattern classifiers.
2.	To learn about unsupervised pattern classifiers.
3.	To familiarize about different feature extraction techniques.
4.	To explore the role of Hidden Marko model and SVM in pattern recognition.
5.	To study the application of Fuzzy logic and genetic algorithms for pattern classifier.

UNIT – I	PATTERN CLASSIFIER	9

Overview of Pattern recognition – Discriminant functions – Supervised learning – Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach – Pattern classification by distance functions – Minimum distance pattern classifier.

UNIT – II	CLUSTERING	9

Clustering for unsupervised learning and classification – Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT – III	FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION	9

Principle component analysis, Independent component analysis, Linear discriminant analysis, Feature selection through functional approximation – Elements of formal grammars, Syntactic description – Stochastic grammars – Structural Representation, Case Study.

UNIT – IV	HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE	9

State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection, Case Study.

UNIT – V	RECENT ADVANCES	9

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.

Total Instructional hours: 45

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Course Outcomes : Students will be able to	
CO1	Outline the concepts of supervised classifiers.
CO2	Outline the concepts of Clustering.
CO3	Classify the data and identify the patterns.
CO4	Make use of feature set and select the features from given data set.
CO5	Apply fuzzy logic and genetic algorithms for classification problems.

Reference Books	
1.	Andrew Webb, “Stastical Pattern Recognition”, Arnold publishers, London, 1999.
2.	C.M.Bishop, “Pattern Recognition and Machine Learning”, Springer, 2006.
3.	M. Narasimha Murthy and V. Susheela Devi, “Pattern Recognition”, Springer, 2011.
4.	Menahem Friedman and Abraham Kandel, “Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches”, World Scientific publishing Co. Ltd, 2000.
5.	Robert J.Schalkoff, “Pattern Recognition Statistical, Structural and Neural Approaches”, John Wiley & Sons Inc., New York, 1992.
6.	R.O.Duda, P.E.Hart and D.G.Stork, “Pattern Classification”, John Wiley, 2001.
7.	S.Theodoridis and K.Koutroumbas, “Pattern Recognition”, Academic Press, 4th Ed., 2009.

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M.E.	M19AET102 - EMBEDDED SYSTEM DESIGN (Common to AE and VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce the overview, design metrics and methodology of embedded systems.
2.	To introduce architecture of single purpose processor.
3.	To understand various protocols of embedded system.
4.	To understand the State machine models.
5.	To introduce software development tools.

UNIT – I	EMBEDDED SYSTEM OVERVIEW	9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT – II	GENERAL AND SINGLE PURPOSE PROCESSOR	9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer‟s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT – III	BUS STRUCTURES	9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT – IV	STATE MACHINE AND CONCURRENT PROCESS MODELS	9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-: Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

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UNIT – V	EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	9
Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Explain the design challenges and basic metrics of embedded system.
CO2	Explain the architecture and pipelining process.
CO3	:Analyse different protocols.
CO4	Examine the state machine and design process models.
CO5	Outline embedded software development tools and RTOS.

Reference Books	
1.	Bruce Powel Douglas, “Real time UML, second edition : Developing efficient objects for embedded systems”, Pearson Education, 3rd Edition, 1999.
2.	Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education, 2002.
3.	Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons, 2002.
4.	Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.

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Professional Elective - V

M.E.	M19VDE302 - MEMS and NEMS (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To introduce the concepts of micro-electromechanical devices.
2.	To know the fabrication process of Microsystems.
3.	To know the design concepts of micro sensors.
4.	To know the design concepts of micro actuators.
5.	To familiarize concepts of quantum mechanics and nano systems.

UNIT – I	OVERVIEW	9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT – II	MEMS FABRICATION TECHNOLOGIES	9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT – III	MICRO SENSORS	9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT – IV	MICRO ACTUATORS	9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

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UNIT – V	NANOSYSTEMS AND QUANTUM MECHANICS	9
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Outline the concepts of micro-electromechanical devices.
CO2	Explain the fabrication process of Microsystems.
CO3	Design the concepts of micro sensors.
CO4	Design the concepts of micro actuators.
CO5	Explain concepts of quantum mechanics and nano systems.

Reference Books	
1.	Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006.
2.	Marc Madou, “Fundamentals of Micro-fabrication”, CRC Press, 1997.
3.	Stephen D. Senturia, “Micro system Design”, Kluwer Academic Publishers, 2001.
4.	Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures”, CRC Press, 2002.
5.	Tai Ran Hsu , “MEMS and Microsystems Design and Manufacture”, Tata McGraw Hill, 2002.

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M.E.	M19VDE303 – HARDWARE - SOFTWARE CO-DESIGN (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To acquire the knowledge about system specification and modelling.
2.	To learn the formulation of partitioning.
3.	To learn the co-synthesis.
4.	To study the different technical aspects about prototyping and emulation.
5.	To introduce the design specification and verification.

UNIT – I	SYSTEM SPECIFICATION AND MODELLING	9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT – II	HARDWARE / SOFTWARE PARTITIONING	9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT – III	HARDWARE / SOFTWARE CO-SYNTHESIS	9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT – IV	PROTOTYPING AND EMULATION	9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems.

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UNIT – V	DESIGN SPECIFICATION AND VERIFICATION	9
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Outline the system specification and modelling.
CO2	Explain the partitioning and scheduling Algorithm.
CO3	Explain the co-synthesis algorithm.
CO4	Compare various architectures od prototyping and emulation.
CO5	Analyze about the design specification and validate its functionality by simulation.

Reference Books	
1.	Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design”, Kaufmann Publishers, 2001.
2.	Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
3.	Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.

EXCELLENCE BEYOND EXPECTATIONS COIMBATORE

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M.E.	M19AEE205 – ROBOTICS (Common to AE and VLSI)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand robot locomotion and mobile robot kinematics.
2.	To understand perception in robotics.
3.	To study mobile robot localization.
4.	To learn the mobile robot mapping.
5.	To study robot planning and navigation.

UNIT – I	LOCOMOTION AND KINEMATICS	9

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability

UNIT – II	ROBOT PERCEPTION	9

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data.

UNIT – III	MOBILE ROBOT LOCALIZATION	9

Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments.

UNIT – IV	MOBILE ROBOT MAPPING	9

Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM –extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fastSLAM algorithm.

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UNIT – V	PLANNING AND NAVIGATION	9
Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Explain robot locomotion, kinematics models and constraints.
CO2	Analyze the vision algorithms for robotics
CO3	Test for robot localization techniques
CO4	Test for robot mapping techniques
CO5	Analyze the planning and exploration algorithms

Reference Books	
1.	Gregory DudekandMichael Jenkin, “Computational Principles of Mobile Robotics”, Second Edition, Cambridge University Press, 2010.
2.	Howie Choset etal., “Principles of Robot Motion : Theory, Algorithms and Implementations”, A Bradford Book, 2005.
3.	Maja J. Mataric, “The Robotics Primer”, MIT Press, 2007.
4.	Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, “Introduction to autonomous mobile robots”, Second Edition, MIT Press, 2011.
5.	Sebastian Thrun, Wolfram Burgard, and Dieter Fox, “Probabilistic Robotics”, MIT Press, 2005.

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M.E.	M19VDE304 - SOLID STATE DEVICE MODELLING AND SIMULATION (Common to VLSI & AE)	T	P	TU	C
		3	0	0	3

Course Objectives	
1.	To understand the basic concept of device modelling.
2.	To learn concept of device modelling.
3.	To learn multistep method.
4.	To learn the mathematical techniques in device simulations.
5.	To study about the simulation of devices.

UNIT – I	MOSFET DEVICE PHYSICS MOSFET	9

capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT – II	DEVICE MODELLING	9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT – III	MULTISTEP METHODS	9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT – IV	MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS	9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

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UNIT – V	SIMULATION OF DEVICES	9
Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.		
		Total Instructional hours: 45

Course Outcomes : Students will be able to	
CO1	Analyse the circuits using basic modelling, advanced modelling and parasitic BJT parameters.
CO2	Analyse the various device modelling techniques and newton raphson method.
CO3	Apply and determine the Multistep methods and stiff system equation.
CO4	Analyse the mathematical equations involved in device simulation.
CO5	Explain the small signal analysis of MOS capacitor.

Reference Books	
1.	Arora, N., “MOSFET Modelling for VLSI Simulation”, Cadence Design Systems, 2007.
2.	Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall., 1975.
3.	Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modelling and Circuit Simulation”, Wiley-Interscience., 1997.
4.	Grasser, T., “Advanced Device Modelling and Simulation”, World Scientific Publishing Company, 2003.
5.	Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer- Verlag, 1984.
6.	Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modelling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.

BoS Chairman

M.E.	M19VDP301 - PROJECT WORK (PHASE I)	T	P	TU	C
		0	12	0	6

Course Objectives	
1.	To enable a student to do an individual project work this may involve design, modelling, simulation and/or fabrication.
2.	To analyse a problem both theoretically and practically.
3.	To motivate the students to involve in research activities leading to innovative solutions for industrial and societal problems.

COURSE DESCRIPTION

Project work shall be carried out by each and every individual student under the supervision of a faculty of this department. A student may however, in certain cases, be permitted to work for the project in association with other departments or in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist from the organization. The student shall meet the supervisor periodically and attend the periodic reviews for evaluating the progress.

Project work will be carried out in two phases, Phase-I during the third semester and Phase-II during the final semester. Phase-I shall be pursued for a minimum of 12 periods per week and Phase – II in 24 periods per week. In each phase, there will be three reviews for continuous internal assessment and one final review and viva voce at the end of the semesters. The Project Report prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

Course Outcomes : Students will be able to	
CO1	Identify the area, narrow dine the problem and understand the problem thoroughly and provide an appropriate solution.
CO2	Show the systematic literature survey which helps to build the knowledge in the chosen field by using the existing journal references
CO3	Construct a mathematical model for the system under study.
CO4	Choose and get proficiency over the software for simulation and analysis.
CO5	Utilize the findings of the phase I work in conferences/journals.

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Semester - IV

M.E.	M19VDP401 - PROJECT WORK (PHASE II)	T	P	TU	C
		0	24	0	12

Course Objectives	
1.	To enable a student to do an individual project work which may involve design, modelling, simulation and/or fabrication
2.	To analyse a problem both theoretically and practically.
3.	To motivate the students to involve in research activities leading to innovative solutions for industrial and societal problems.

COURSE DESCRIPTION:

Project work shall be carried out by each and every individual student under the supervision of a faculty of this department. A student may however, in certain cases, be permitted to work for the project in association with other departments or in an Industrial/Research Organization, on the recommendation of the Head of the Department. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist from the organization. The student shall meet the supervisor periodically and attend the periodic reviews for evaluating the progress.

Project work will be carried out in two phases, Phase-I during the third semester and Phase-II during the final semester. Phase-II shall be pursued for 24 periods per week. In phase II also, there will be three reviews for continuous internal assessment and one final review and viva voce at the end of the semesters. The Project Report prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted to the concerned department.

Course Outcomes : Students will be able to	
CO1	Develop the project model for Phase II
CO2	Apply modern engineering tools for simulation, analysis and Solution
CO3	Evaluate the findings of the project by attending conference and communicate to journals for publication
CO4	Take part in Presentation/ Technical Discussion
CO5	Improve the continuous learning in new practices, principles and techniques in Electronics area.

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